A Novel Programmable Delay Line for VLSI Systems

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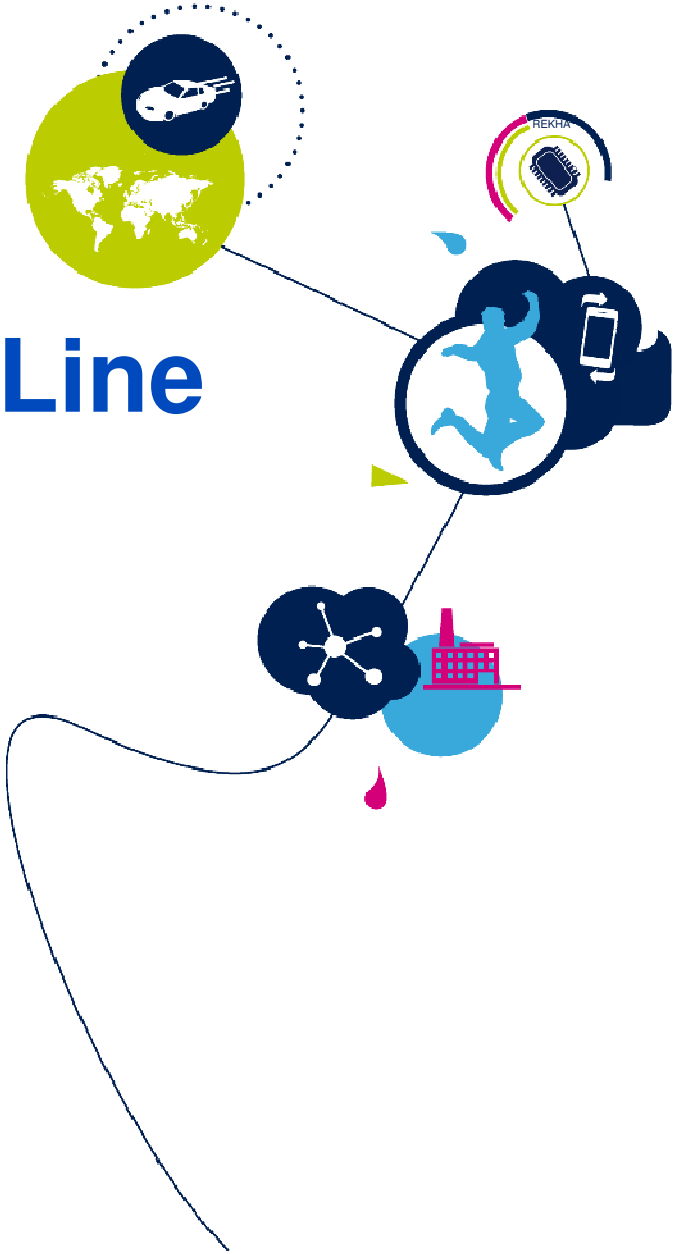

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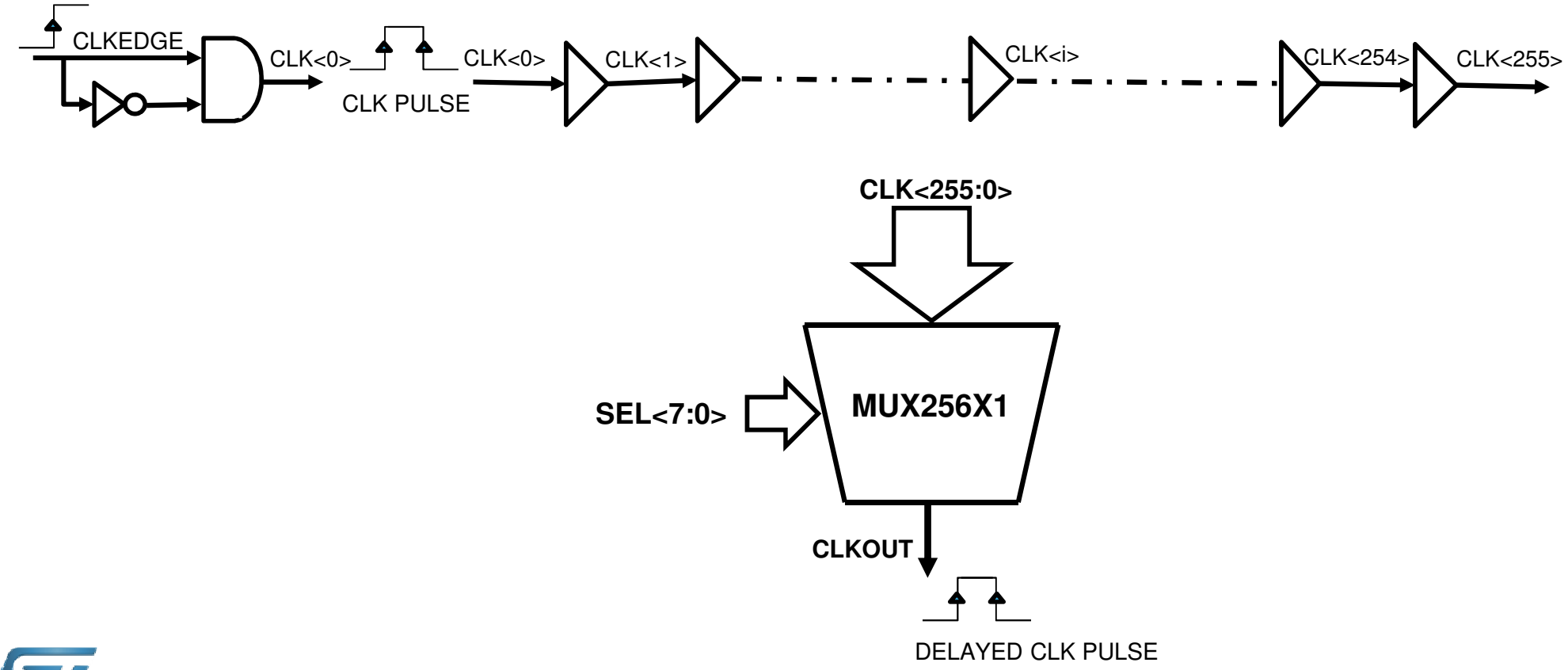
Agenda

- Motivation
- Contemporary Architecture
- Applications of Delay lines
- Proposed Novel Programmable Delay Architecture
- Simulation Results
- Key Benefits
- Conclusion

Motivation

- In digital ASICs, controlled clock delay finds many applications.
- Several buffers are required for large absolute delays
- Along with accuracy, granular control is also desired
- Large buffers chains contribute to substantial Leakage power
- On chip Delay variation is seen among the delay elements
- The delay selection multiplexor has high fan-in

Contemporary Architecture



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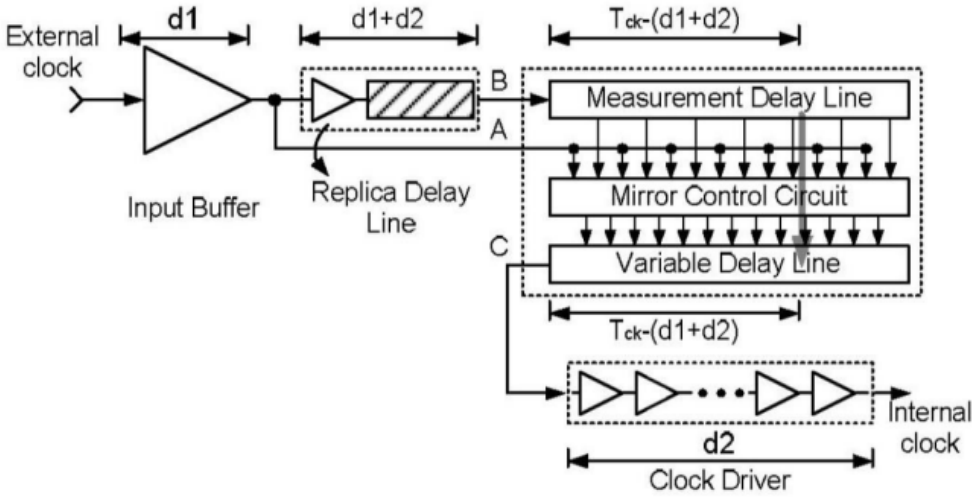
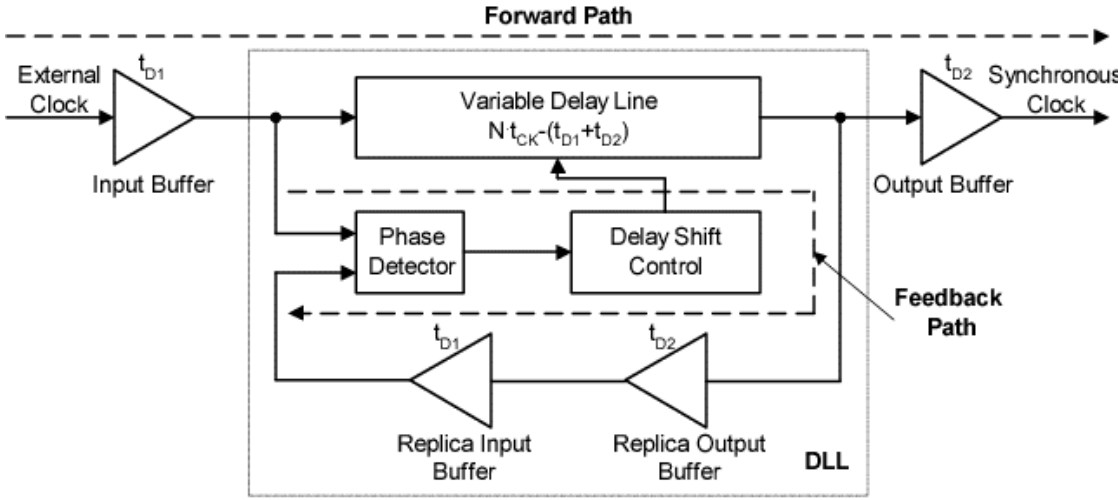
Applications of Delay Lines

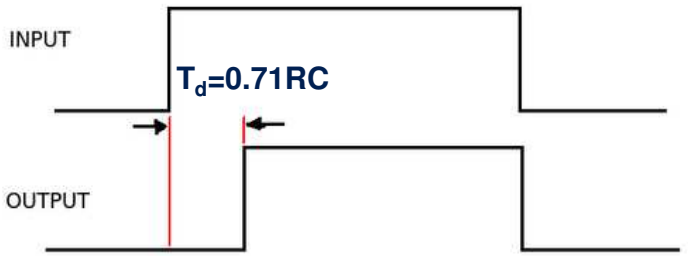
- **Synchronous Mirror Delay Circuit**



- **Delay Locked Loop**



- **Clock-less, RC free, Delay**



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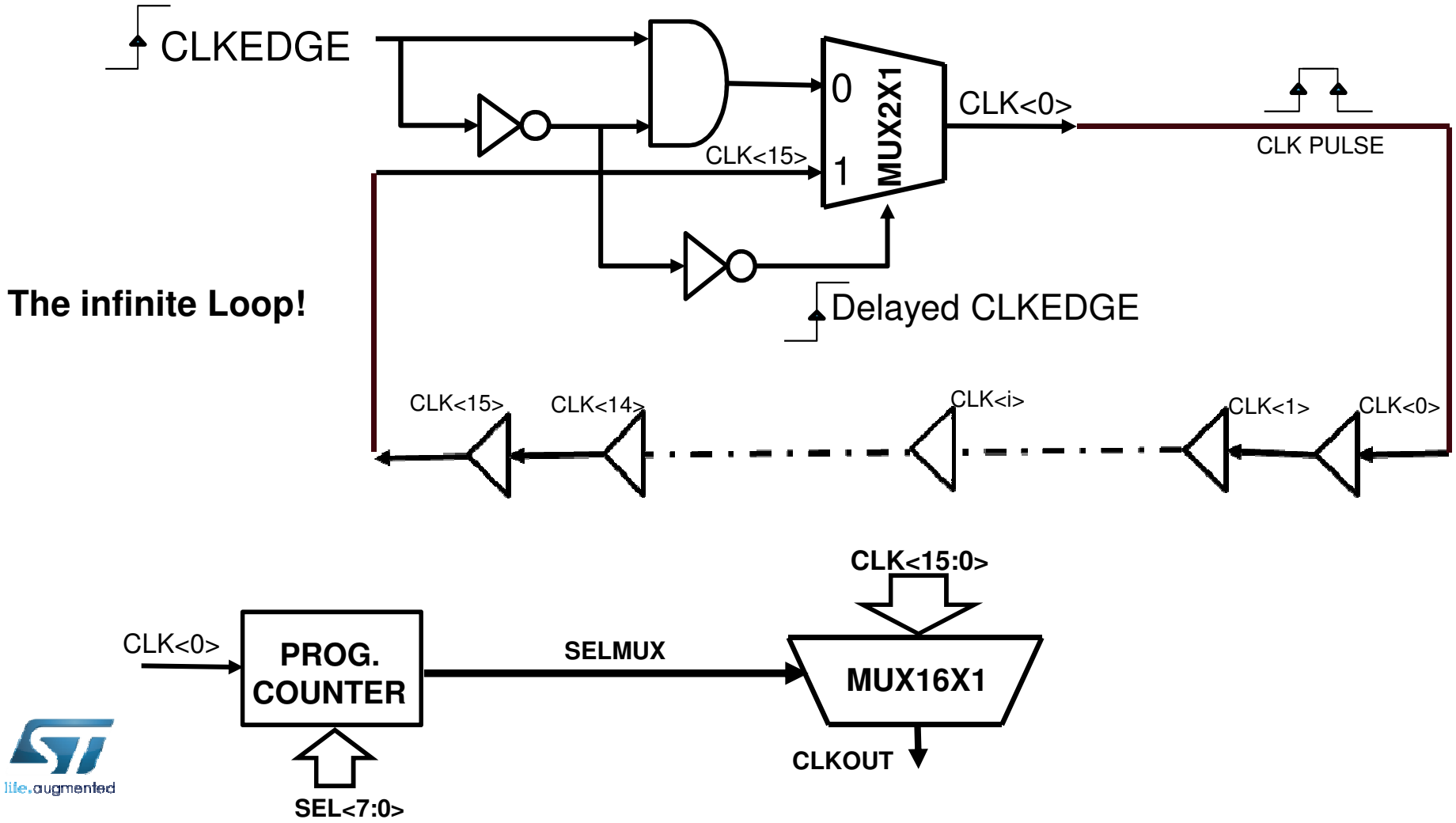
Proposed Novel Programmable Delay Architecture



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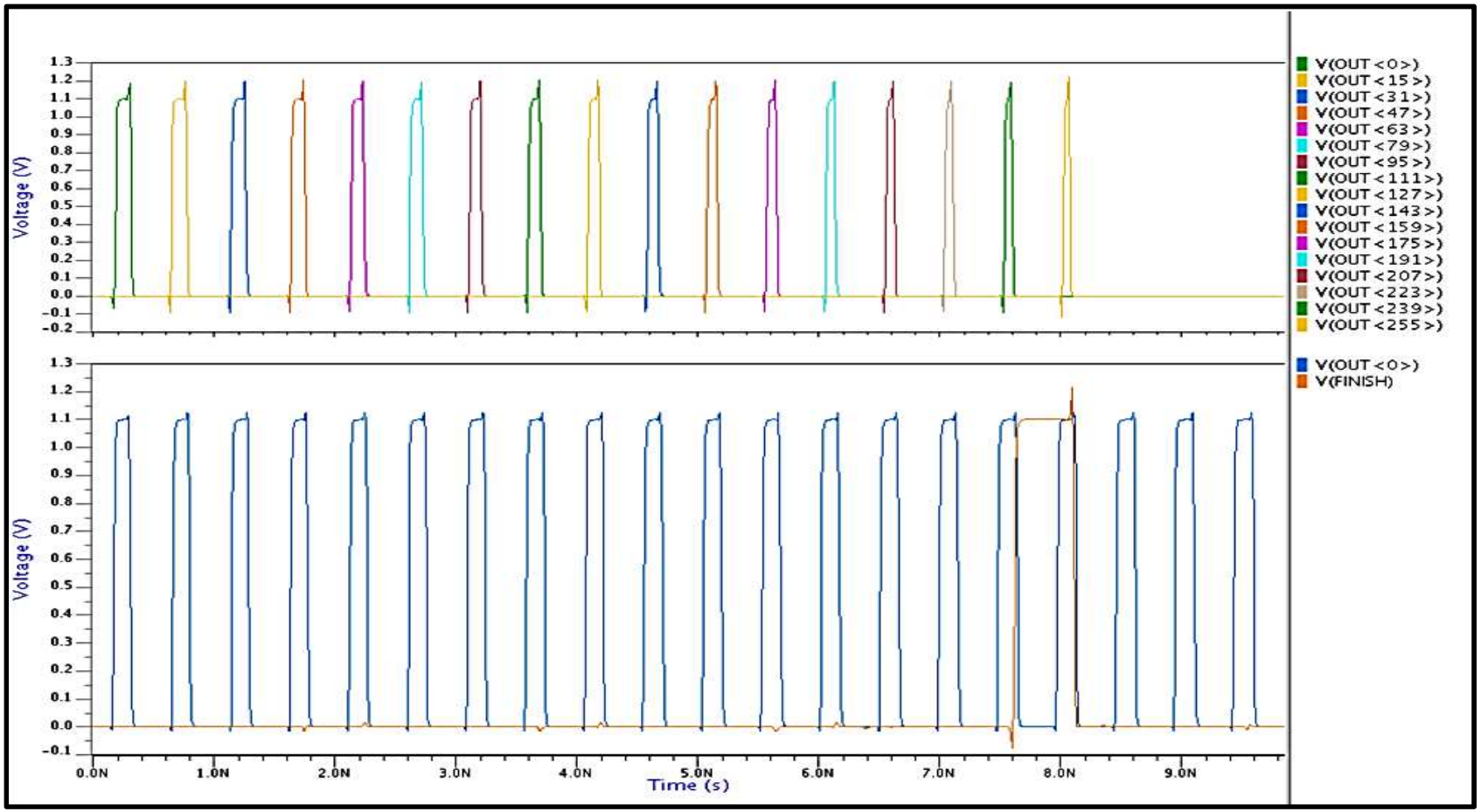
Simulation Results: Delay Comparisons

256 Buffers ⇨

16 Buffers ⇨



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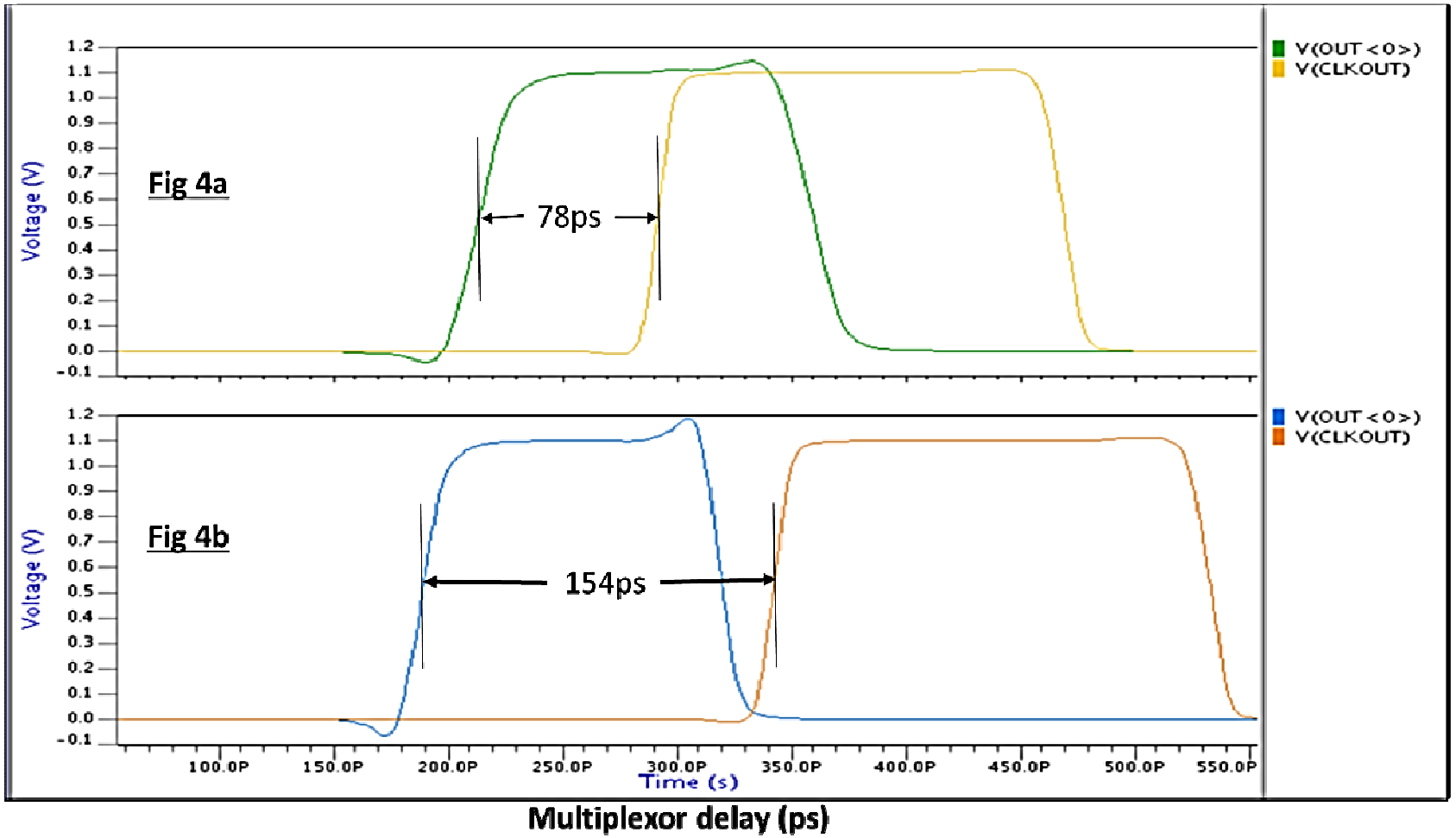
Simulation Results: Selection Delays

16 Buffers ⇨

256 Buffers ⇨



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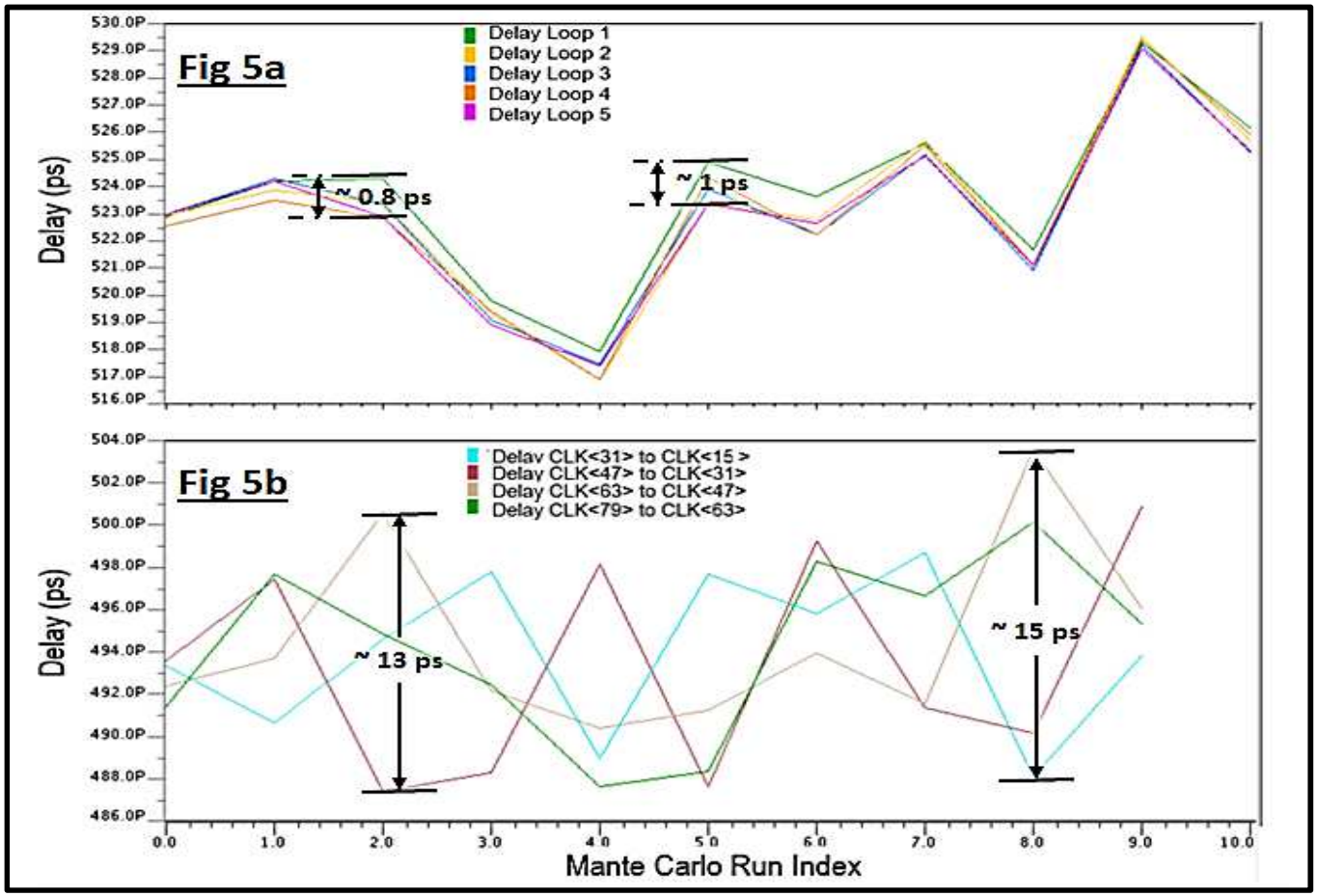
Simulation Results: Delay Variation

16 Buffers ⇨

256 Buffers ⇨



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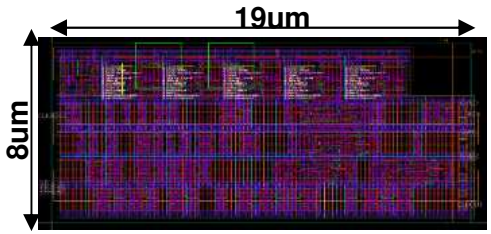
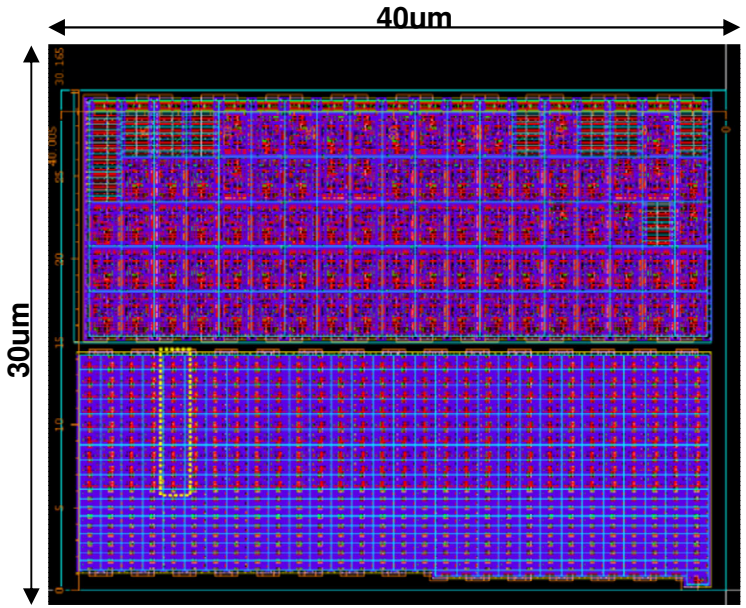
Silicon Area Comparison

Area: 8X advantage





Proposed 256 buffer delay line:

- area = 19*8 = 0.00152um2

Conventional 256 buffer delay line:

- area = 30* 40 = 0.012um2

Figure of Merit Comparison (in 28nm FDSOI)

	Conventional	Proposed	Gain
Area (in um^2)	1200	150	8
Leakage Power (in uA)	22.11	2.29	10
MUX delay (in pS)	154	78	2
Delay variation (in pS)	15	1	15

Key Benefits

- Use of lower number of buffers to achieve identical delay
- Low area and leakage power very useful in newer technologies
- Very low local variation across process corners
- Scalable to higher delays using minimal overheads
- Modular structure makes architecture implementation automable
- Plug and play usage in existing systems

Conclusion

- Design methodology for design of a programmable delay line circuit is presented
- A compact delay line circuit is demonstrated to generate multiple phases of clock
- A comparison of Figures-of-Merits with the conventional architecture reveals significant gain in terms of area, leakage power and variability
- This approach can be extended to arbitrary large delay generation by dynamic duty cycle correction

Thank You

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