Frequency-Dependent Target Impedance Method Fulfilling Both Average and Dynamic Voltage Drop Constraints

Jun Chen, Masanori Hashimoto

Department of Information Systems Engineering

Osaka University, Japan

大阪大学
OSAKA UNIVERSITY

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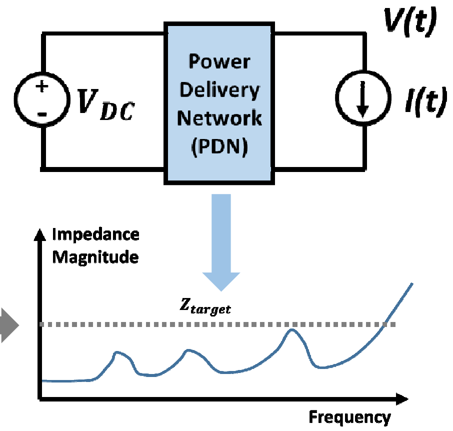
Agenda

- **Background of Target Impedance**
  - Challenges for target impedance
  - Contribution of this work
- **Frequency-Dependent Target Impedance**
  - Target impedance deriving flow
  - Magnitude equivalent frequency (MEF)
  - Synthesize target impedance
- **Experiment Results**
- **Conclusion**

Background of target impedance

PDN uses target impedance to ensure maximum allowed voltage drop[1]



$$Z_{target} = \frac{V_{allowed\_drop}}{I}$$

Flat Z_{target} is increasingly difficult to meet

Cause under- or over-designed PDN.

Frequency-dependent $Z_{target}(f)$ is an open problem.

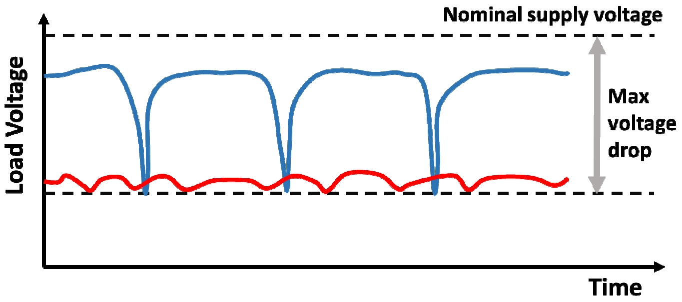
Requirement and challenge

Consider average and dynamic voltage drop constraints.

Associate frequency-domain Z_{target} and time-domain I, V.

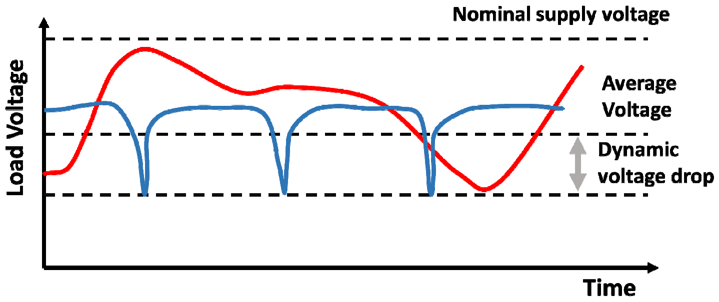
[1] L. D. Smith, et al., "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology", IEEE Trans. Advanced Packaging, vol. 22, no. 3, pp. 284-291, 1999.

Average and dynamic voltage drop constraints are NOT well considered in previous work.



Given one voltage drop constraint,
PDN can be **over- or under-designed**.
blue needs more focus on dynamic drop.
red needs more focus on average drop.

Deriving Z_{target} *(f)* using <u>current spectrum</u> and <u>voltage spectrum</u>[2] has limitation.



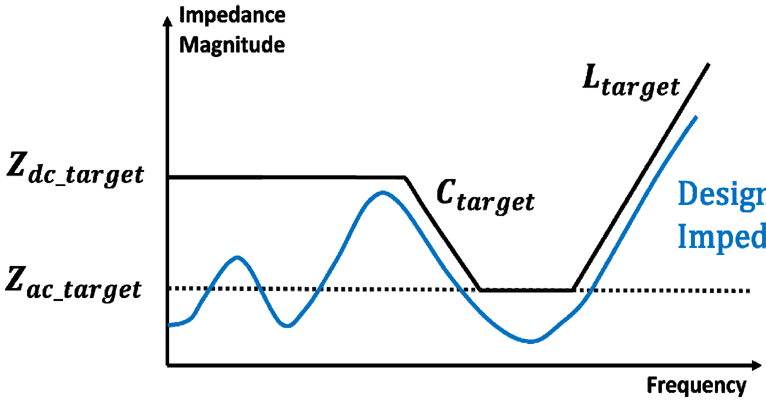
Converting voltage drop constraints to voltage spectrum has many **variations**.
(blue and red with same constraints)
$Z_{target}(f)$ is not unique

[2] D. Oh, Y. Shim, "Power integrity analysis for core timing models", Proc. Int'l Symposium on EMC, pp. 833-838, Aug. 2014.

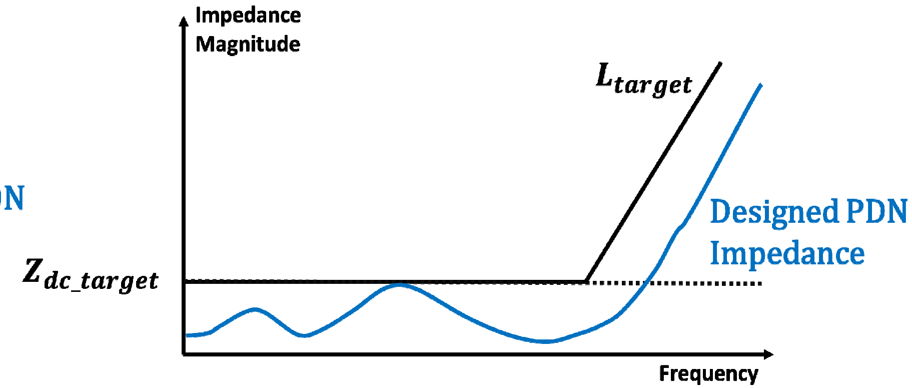
Contribution of this work

1. **Fulfills both average and dynamic voltage drop constraints.**

   Two Z_{target} types for different constraints focus.



Dynamic voltage drop is main design focus



Average voltage drop is main design focus

2. **Associates time-domain *I*, *V* with frequency-domain Z_{target}.**

   By idea of Magnitude Equivalent Frequency (**MEF**).

   Verified result by synthesized Z_{target} circuit.

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Target impedance deriving flow

Inputs:

Load current profile ***I(t)***

Voltage drop constraints V_{avg_allow} and V_{dyn_allow}

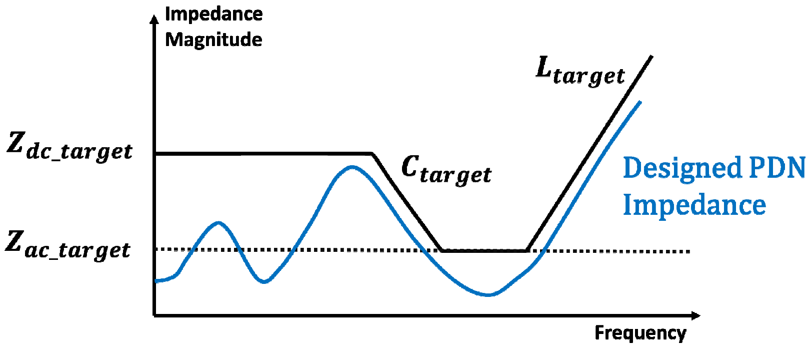
Frequency-dependent Z_{target} is composed of:

Z_{ac_target} : target impedance at middle-high frequency

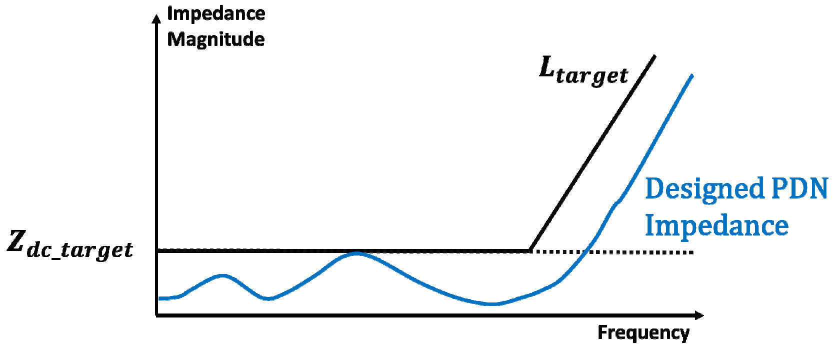
Z_{dc_target} : target impedance at low frequency

C_{target} : target capacitance, min required capacitance

L_{target} : target inductance, max allowed inductance



V_{dyn_allow} **is main design focus**

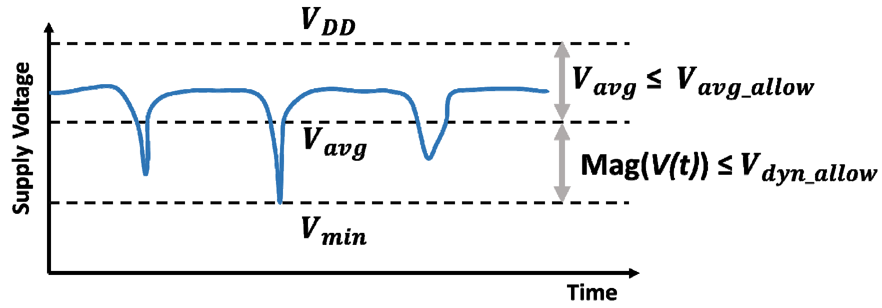


V_{avg_allow} **is main design focus**

Derive Z_{ac_target} and Z_{dc_target}

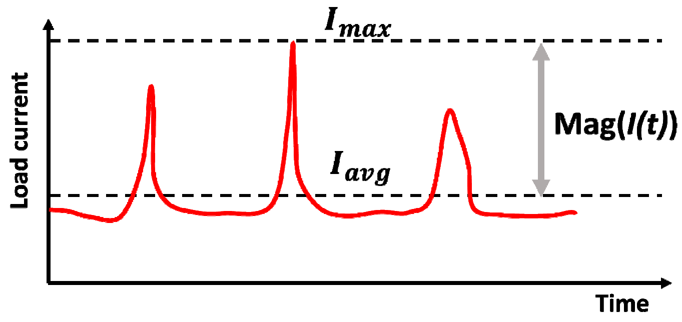
Consider V_{avg_allow} constraints:

$$Z_{dc\_target} = V_{avg\_allow} / I_{avg}$$



Consider V_{dyn_allow} constraints:

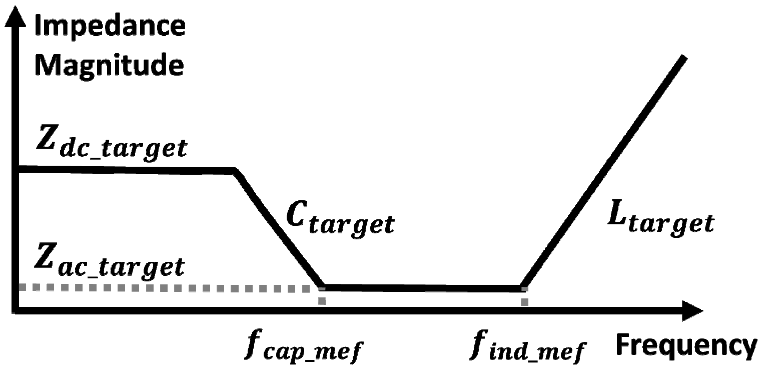
$$Z_{ac\_target} = V_{dyn\_allow} / \text{Mag}(I(t))$$



Result in piecewise Z_{target} shapes:

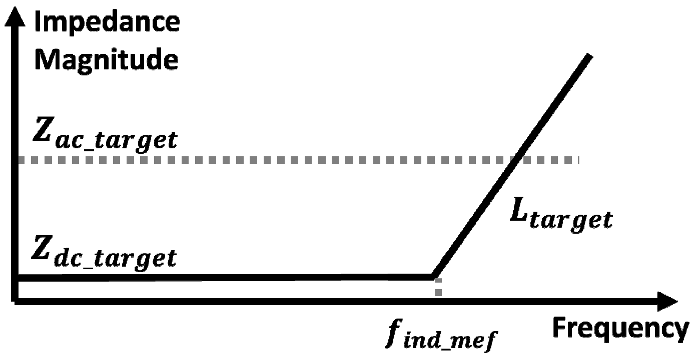
$Z_{ac\_target} < Z_{dc\_target}$

V_{dyn_allow} drop is design focus



$Z_{ac\_target} \geq Z_{dc\_target}$

V_{avg_allow} drop is design focus

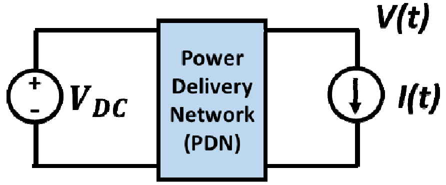


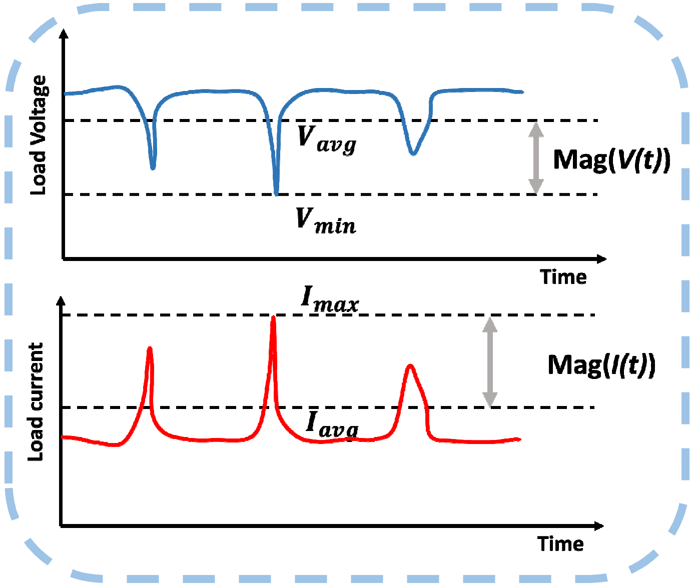
Magnitude equivalent frequency (MEF) I

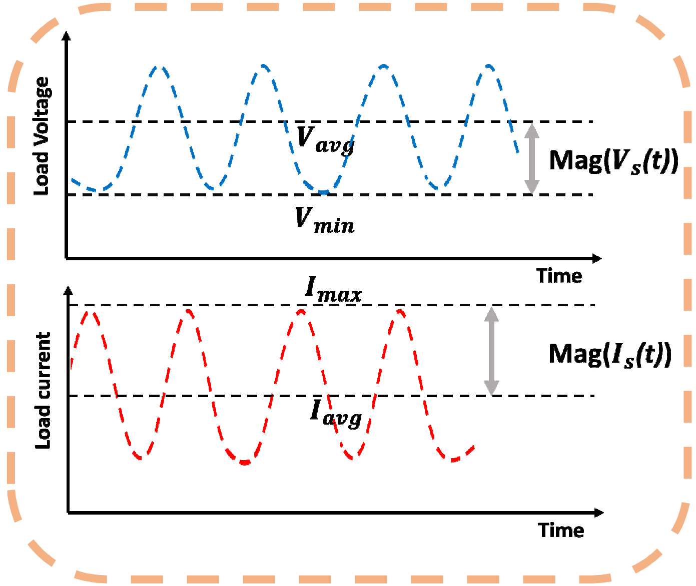
can be represented by

dynamic voltage drop — ***sine*** current with **MEF**

If impedance is
C **dominated**
or
L **dominated**







L dominant impedance example:

Let $\boldsymbol{I_s(t)} = \text{Mag}(\boldsymbol{I(t)}) \sin(2\pi\, f_{MEF}\, t)$, **Mag($\boldsymbol{I_s(t)}$) = Mag($\boldsymbol{I(t)}$)**

Then $\quad \text{Mag}(\boldsymbol{V_s(t)}) = \text{Mag}(L\,\frac{dI_s}{dt}) = \cancel{L}\, 2\pi\, f_{MEF}\, \text{Mag}(\boldsymbol{I(t)})$

Can equal to: $\quad \text{Mag}(\boldsymbol{V(t)}) = \text{Mag}(L\,\frac{dI}{dt}) = \cancel{L}\, \text{Mag}(\frac{dI}{dt})$

***Similar with *C* dominant impedance.**

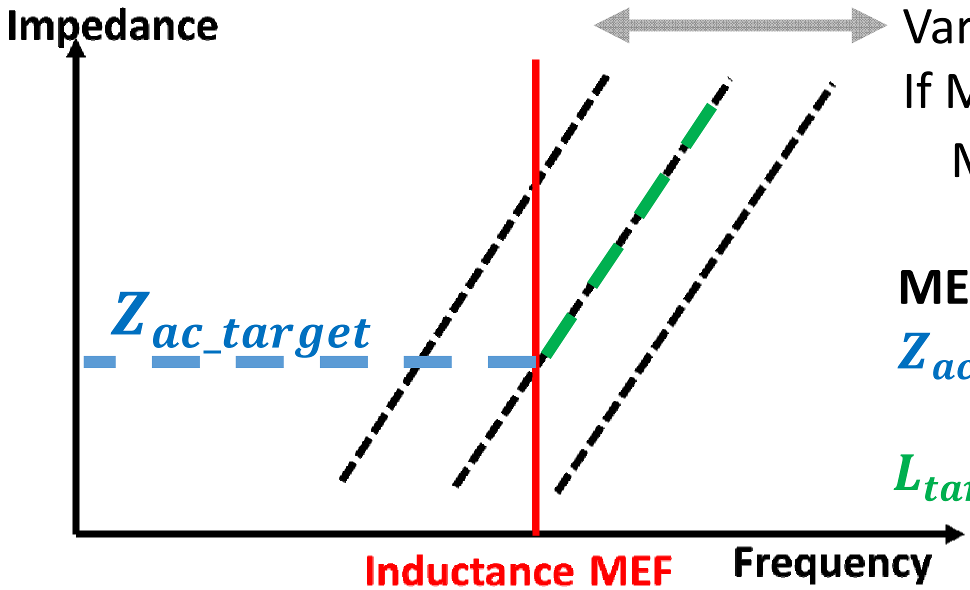
Magnitude equivalent frequency (MEF) II

With different *L* or *C*, MEF sine current can still replay the dynamic voltage drop. (equations still hold with <u>same</u> MEF)

$$\text{Mag}(I_s(t)) = \text{Mag}(I(t))$$
$$\text{Mag}(V_s(t)) = \text{Mag}(V(t))$$

Since *L* and *C* are common coefficient and can be canceled out in equations.

Use MEF to find L_{target} (max allowed inductance):



Varying *L* for an impedance,
If $\text{Mag}(V_s(t)) = V_{dyn\_allow}$ at MEF,
$\text{Mag}(V(t)) = V_{dyn\_allow}$ also holds.

MEF serves as corner frequency of

$$Z_{ac\_target} = V_{dyn\_allow} / \text{Mag}(I(t))$$

$$L_{target} = \frac{Z_{ac\_target}}{2\pi f_{ind\_mef}}$$

Magnitude equivalent frequency (MEF) III

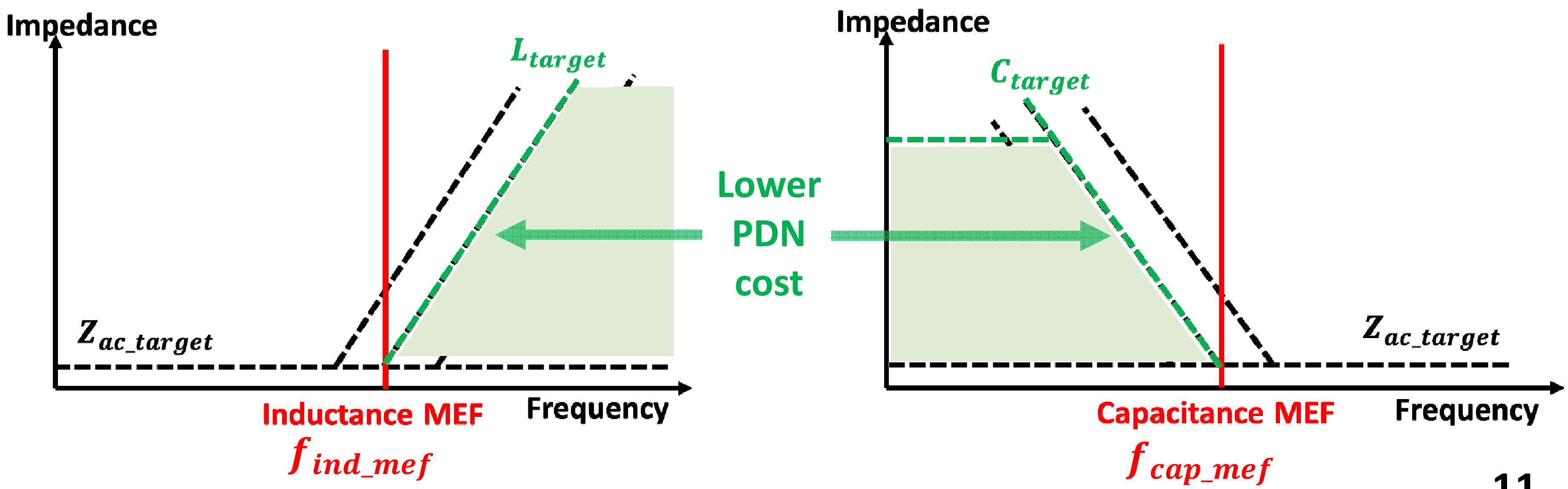
Z_{target} design method is simplified because:

Original current profile (with complex spectrum and profile)

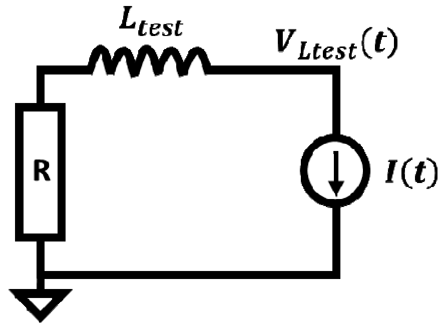
Replaced by **MEF sine** profile (with <u>one</u> spectrum component).

Use **MEF** to find L_{target} (Max allowed inductance).

C_{target} (Min required capacitance).



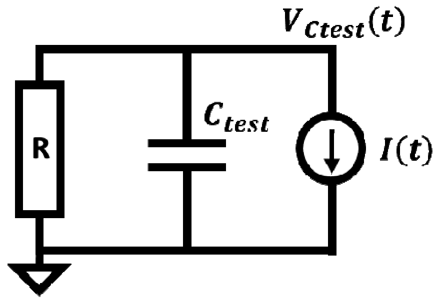
Calculate MEF, L_{target}, and C_{target}



For inductance MEF

Characterization Circuit Setup:

R, L_{test}, C_{test} are known-value parameters.
Form L and C dominant impedance.



For capacitance MEF

Characterization Flow:

Inject $I(t)$ run simulation for $V_{Ltest}(t)$ and $V_{Ctest}(t)$.
Measure Mag($I(t)$) , Mag($V_{Ltest}(t)$), and Mag($V_{Ctest}(t)$).

Inductance MEF is obtained by:

$$f_{ind\_mef} = \frac{\mathrm{Mag}(V_{Ltest}(t))}{\mathrm{Mag}(I(t))} \frac{1}{2\pi L_{test}}$$

Target inductance:

$$L_{target} = \frac{Z_{ac\_target}}{2\pi\, f_{ind\_mef}}$$

Capacitance MEF is obtained by:

$$f_{cap\_mef} = \frac{\mathrm{Mag}(I(t))}{\mathrm{Mag}(V_{Ctest}(t))} \frac{1}{2\pi C_{test}}$$

Target capacitance:

$$C_{target} = \frac{1}{2\pi\, f_{cap\_mef} Z_{ac\_target}}$$

Synthesize Z_{target} circuit

T-shape RLC circuit to track Z_{target}.

Direct using Z_{dc_target}, Z_{ac_target}, C_{target}, L_{target}

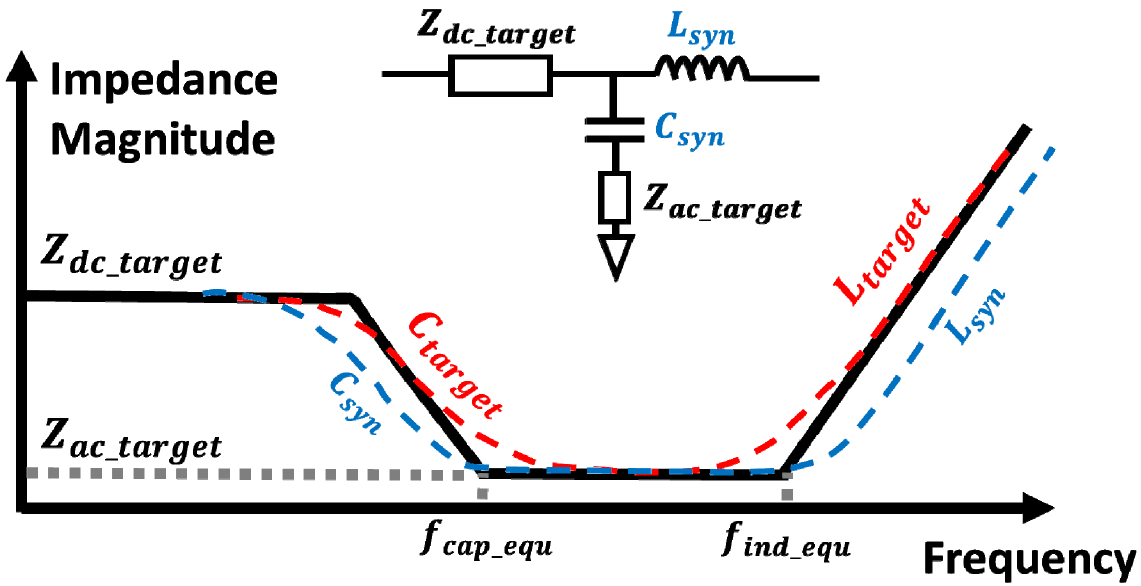
Can violate the voltage drop constraints.

(Actual impedance is larger at **corner frequency**)

In the experiment:

Use larger capacitance and smaller inductance.

Other synthesis method can be applied also.



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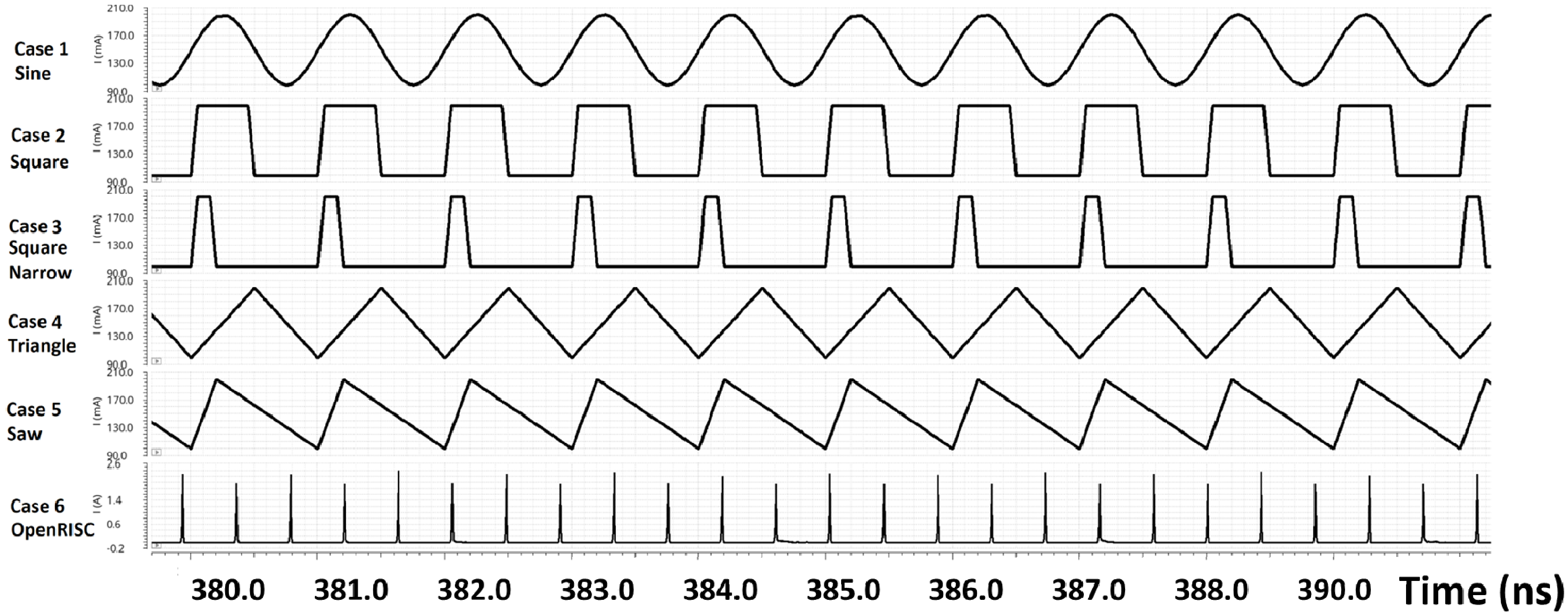
Experiment setup

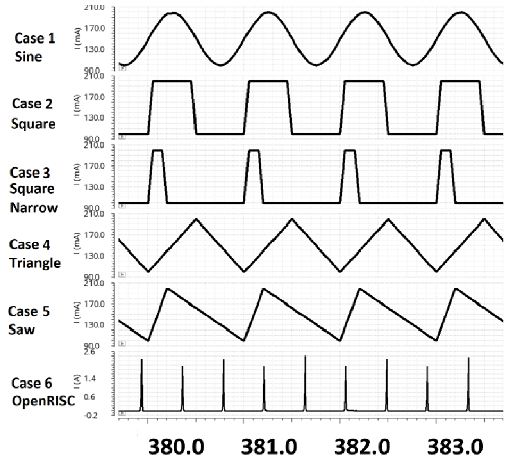
Nominal voltage is 800 mV.

Case 1 : reference 1.0 GHz sine profile.
Case 2 and 3: square current profile to mimic module activations.
Case 4 and 5: triangle current profile to mimic typical digital circuit load.
The constraints are V_{avg_allow}=70 mV and V_{dyn_allow}=10 mV.

Case 6: current profile from OpenRISC operation (15nm Open Cell Lib, 1.2 GHz)
The constraints are V_{avg_allow}=10 mV and V_{dyn_allow}=30 mV.



Experiment results



Measured V_{avg} and V_{min} correlates well with constraints.

Average difference rates are 0.0003% and 0.3%

The derived target impedance associates with current profile.

Wider pulse results in larger C_target

Sharper slope result in smaller L_target

	Z_{dc_target} (mΩ)	Z_{ac_target} (mΩ)	C_{target} (nF)	L_{target} (pH)	V_{avg} (mV)	V_{min} (mV)
Case 1	466.6	200.0	0.8	31.8	730.0	722.5
Case 2	482.7	181.8	1.2	5.0	730.0	722.2
Case 3	608.7	117.6	0.7	5.0	729.9	720.9
Case 4	466.6	200.0	0.6	24.7	730.0	722.5
Case 5	466.6	200.0	0.5	19.8	730.0	722.5
Avg. Diff.	-	-	-	-	0.0003%	0.3%
Case 6	251.9	12.5	0.35	0.01	790.2	760.6
Diff.	-	-	-	-	0.02%	0.07%

Conclusion

- **A new frequency-dependent target impedance method.**
- **Consider both average and dynamic voltage drop constraints.**
- **Associate time domain and frequency domain info with MEF.**
- **Synthesized target impedance correlates well with constraints.**

Q & A