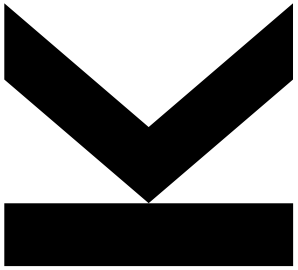
INFLUENCE OF DIFFERENT DIGITAL POWER SUPPLY LAYOUT STYLES ON THE EME OF ICS WITH RESPECT TO PROCESS VARIATIONS



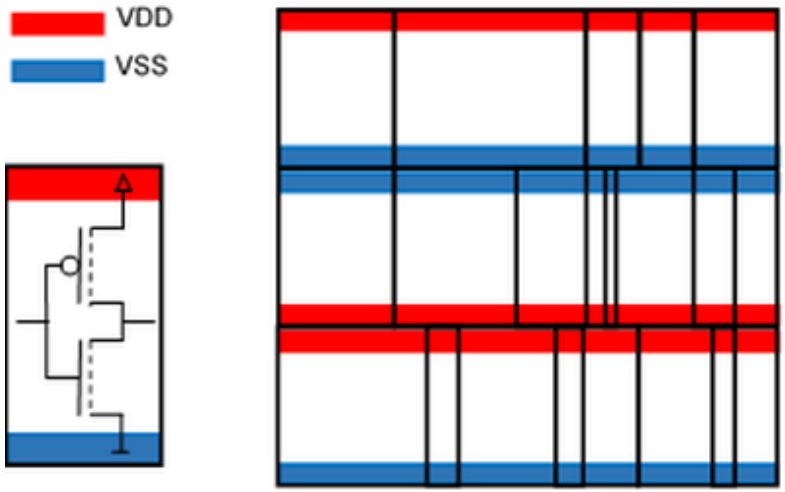
Andreas Rauchenecker and Timm Ostermann
Dept. Energy Efficient Analog Circuits and Systems
Institute for Integrated Circuits
JKU University of Linz/Austria

JOHANNES KEPLER
UNIVERSITÄT LINZ

OVERVIEW

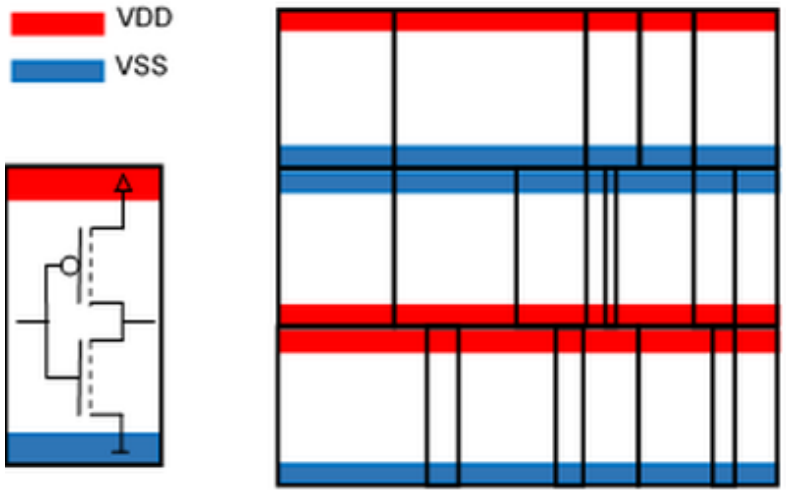
- Standard digital layout
- Test chip
- Process variations
- Measurement
- Conclusion

STANDARD DIGITAL LAYOUT

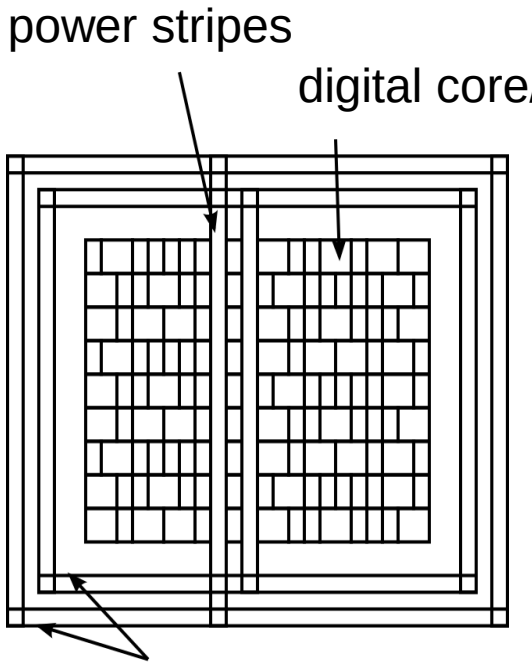


Standard cell/standard cell rows

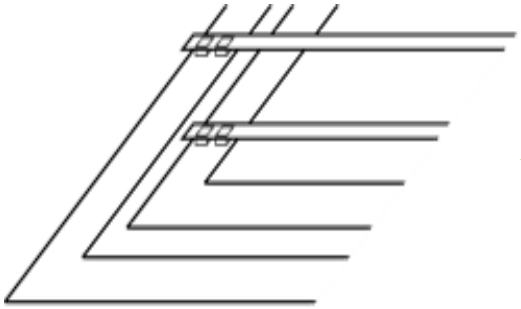
STANDARD DIGITAL LAYOUT

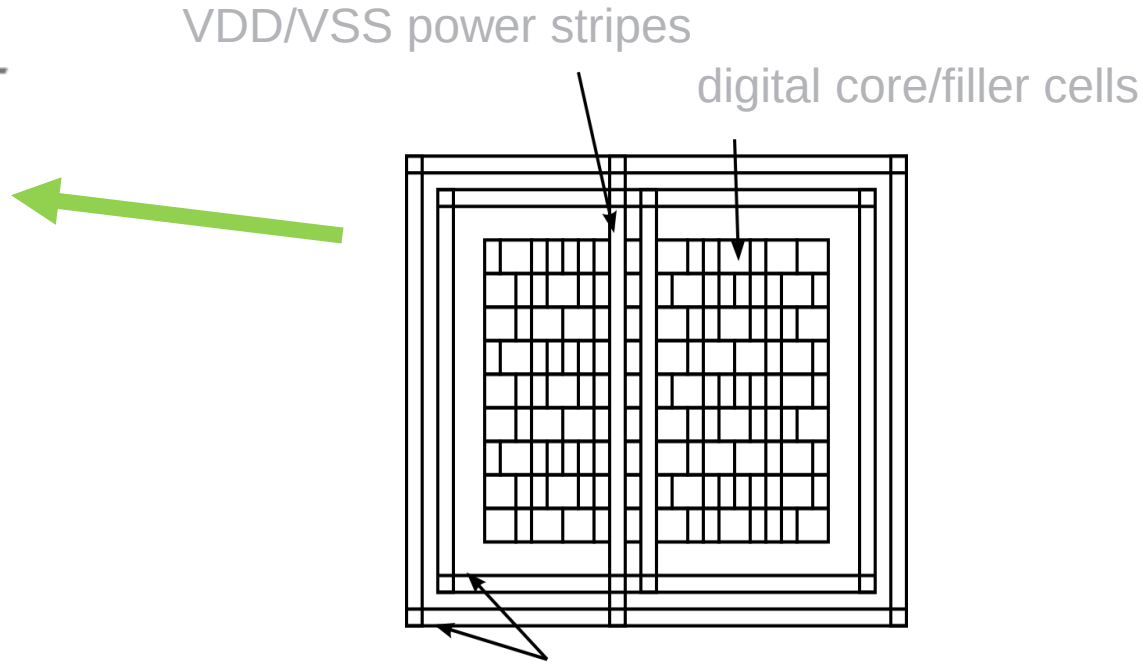


standard cell/standard cell rows

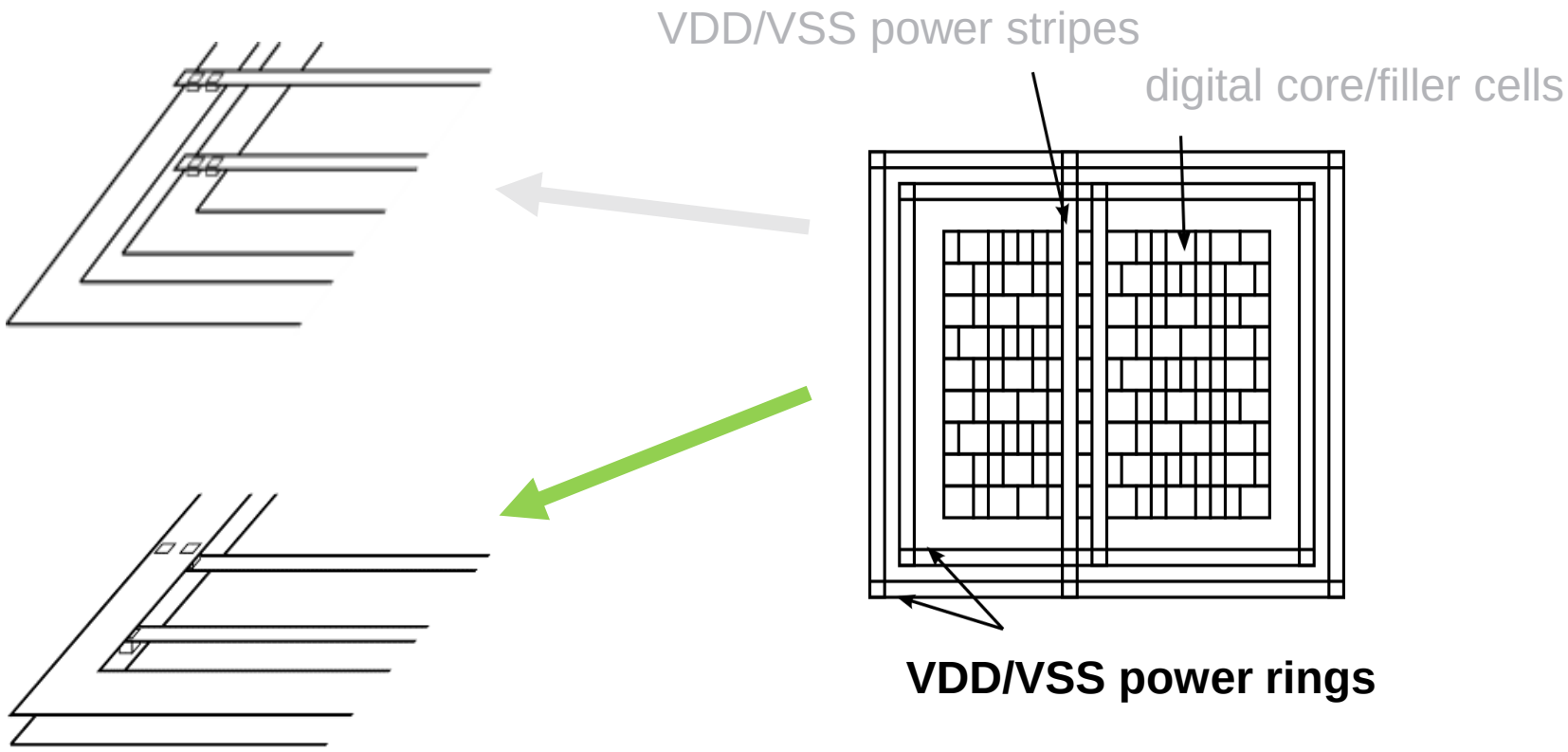


STANDARD DIGITAL LAYOUT



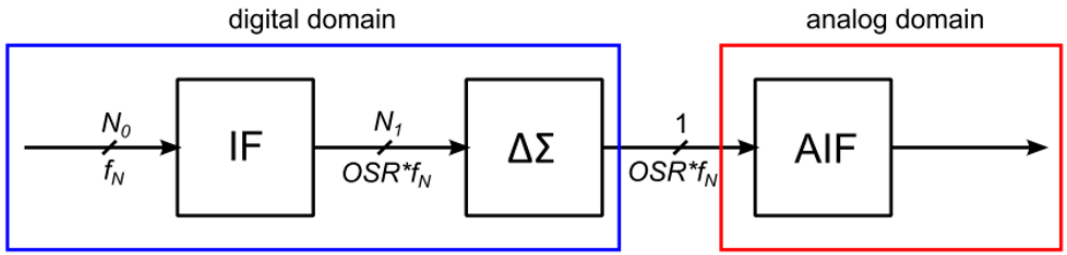


STANDARD DIGITAL LAYOUT



TEST CHIP

Delta sigma digital-to-analog converter (ΔΣ-DAC)



TEST CHIP

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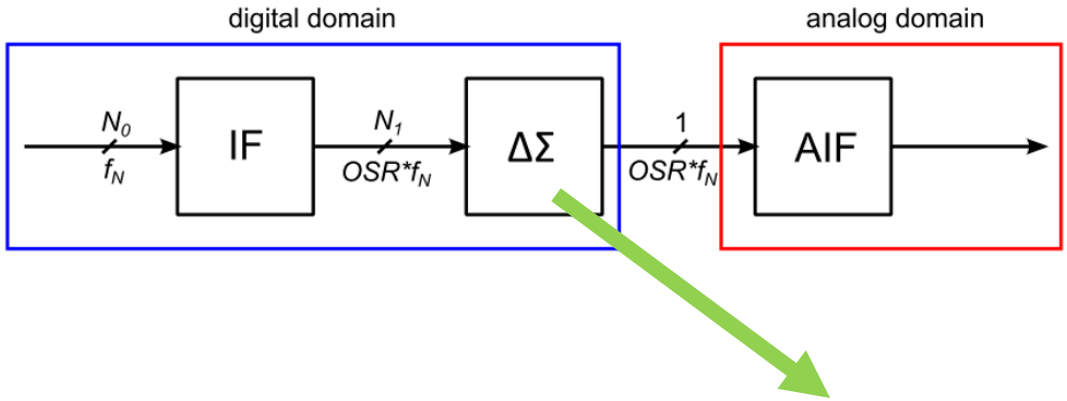
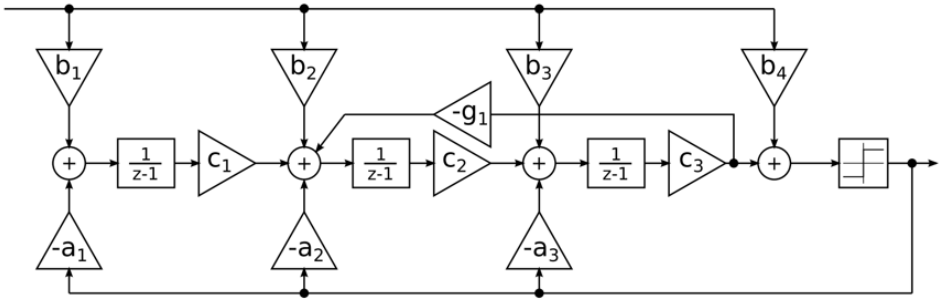


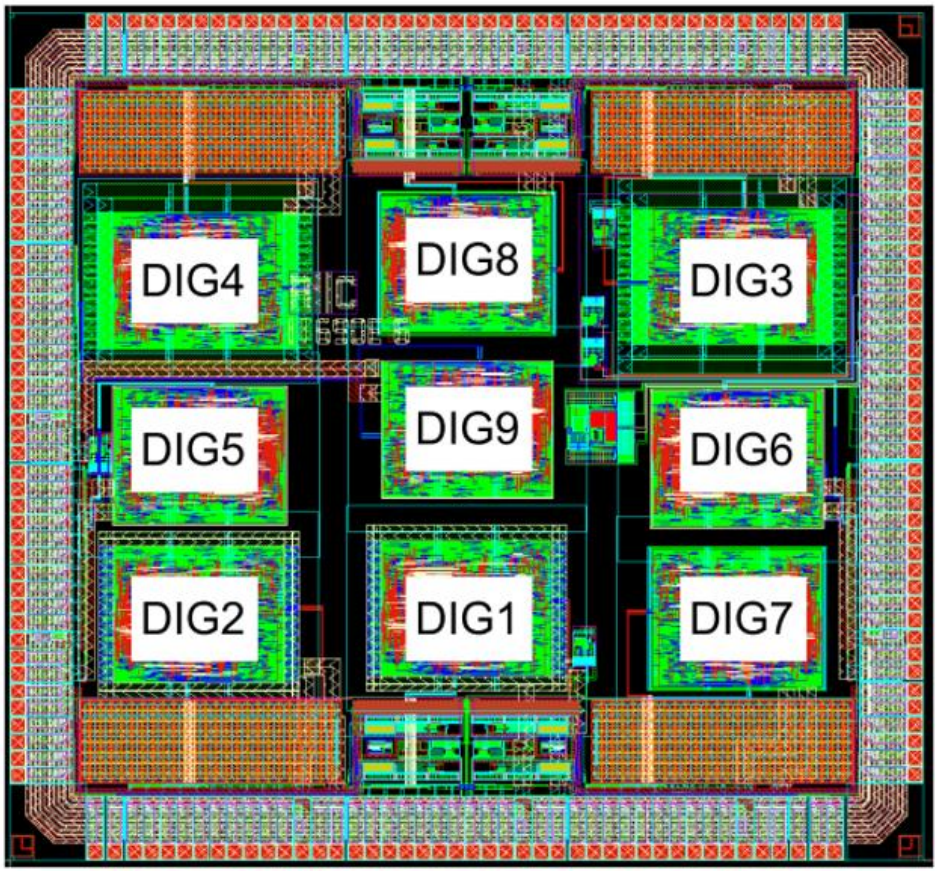
ΔΣ-modulator is realized as a 3rd order CIFB structure

CIFB → cascade-of-integrators feedback



TEST CHIP

Top layout

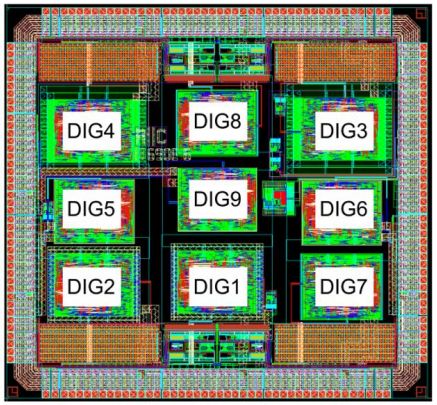


250nm CMOS technology

approx. 32mm²

TEST CHIP

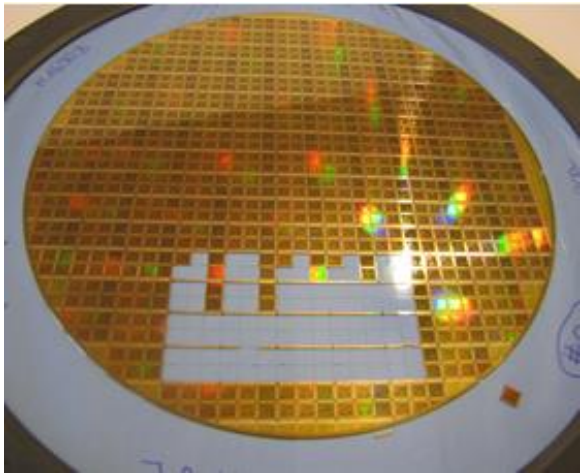
Top layout



Core	Layout Differences			
	Power Ring		*Filler Cells Capacitance*	*Power Stripes*
	Width (VDD or VSS)	*Arrangement*		
DIG1	84µm	stacked	with	yes
DIG2	84µm	stacked	without	yes
DIG3	84µm	flattened	with	yes
DIG4	84µm	flattened	without	yes
DIG5	8.4µm	stacked	with	yes
DIG6	8.4µm	stacked	without	yes
DIG7	8.4µm	flattened	with	yes
DIG8	8.4µm	flattened	without	no
DIG9	2.1µm	stacked	with	yes

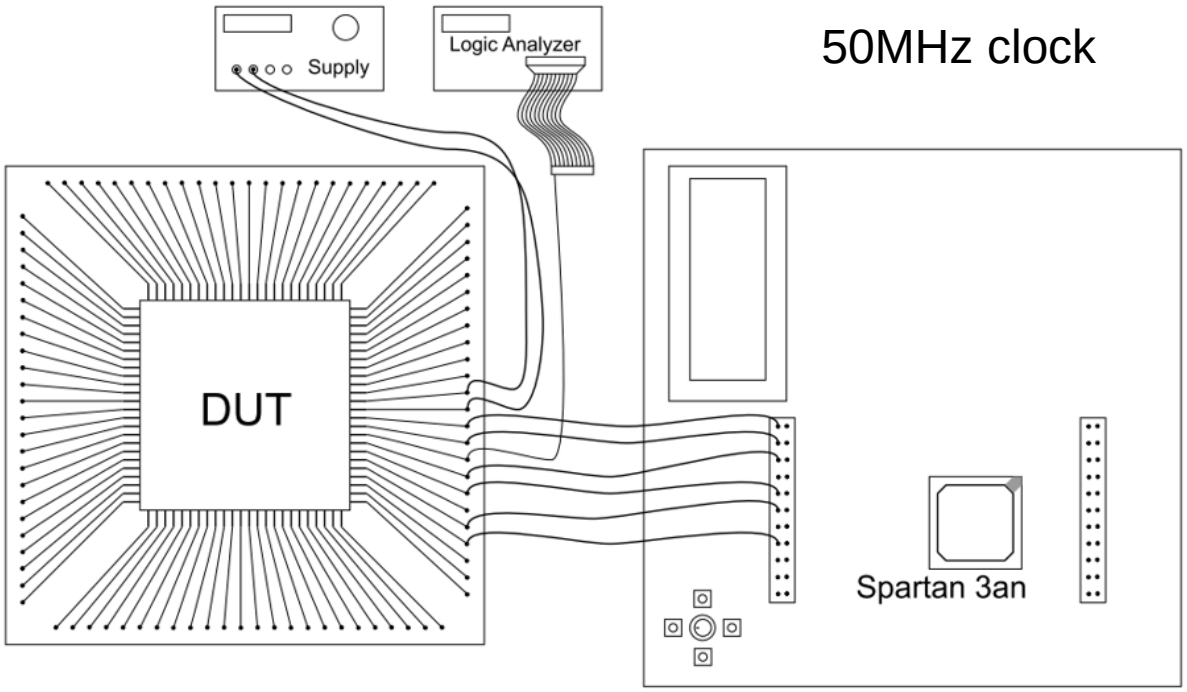
PROCESS VARIATIONS

Split-Lot with 9 different splits (2 wafers each split)

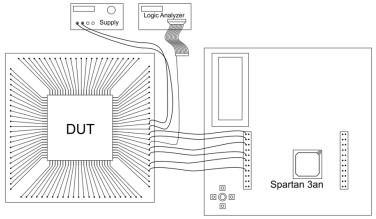


”NOM” → nominal case
”FAST” → MOSFETs in fast process corner
”SLOW” → MOSFETs in slow process corner
”SF” → nMOSFETs slow / pMOSFETs fast
”FS” → nMOSFETs fast / pMOSFETs slow
”HRES” → n-R max., p-R min. values
”LRES” → n-R min., p-R max. values
”LGL” → max. gate length values
”SGL” →min. gate length values

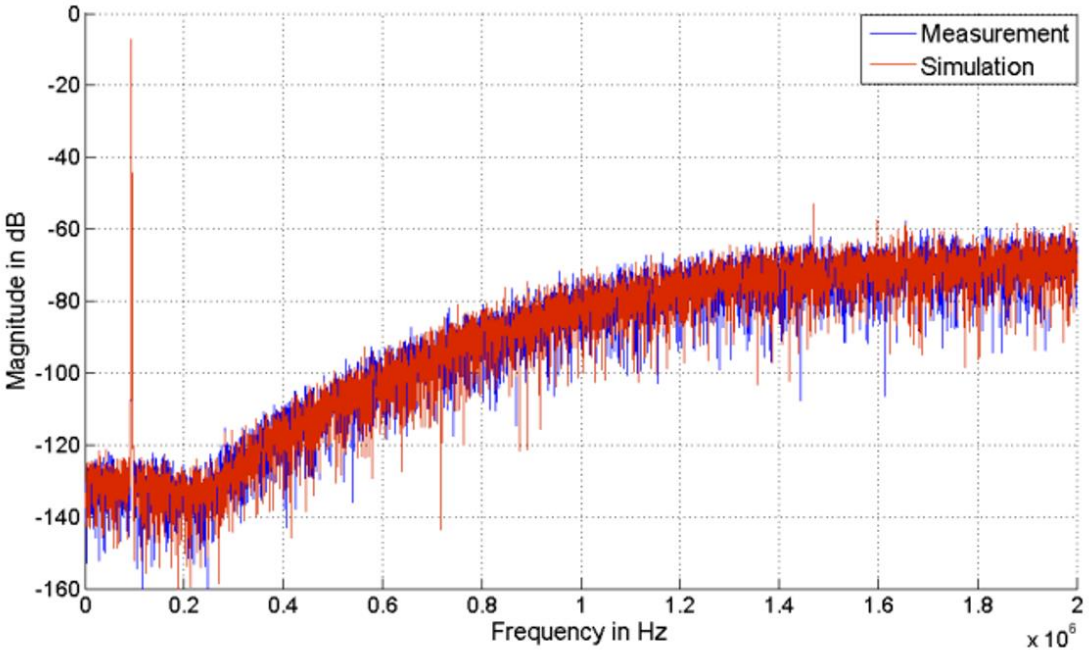
MEASUREMENT
→TEST CHIP FUNCTIONALITY



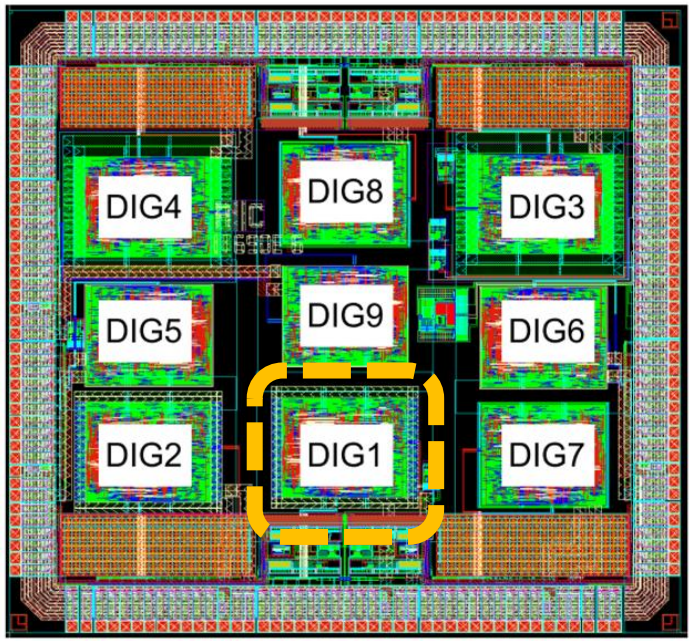
MEASUREMENT
→TEST CHIP FUNCTIONALITY

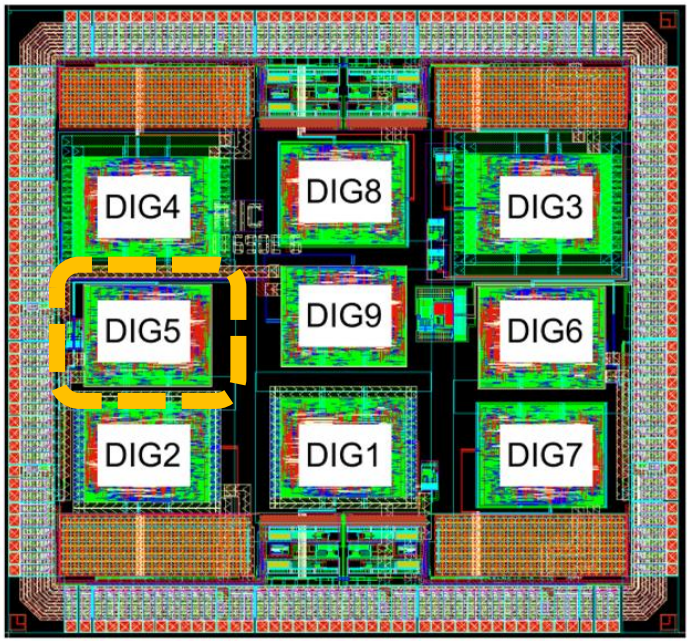


FFT of digital output bitstream



MEASUREMENT



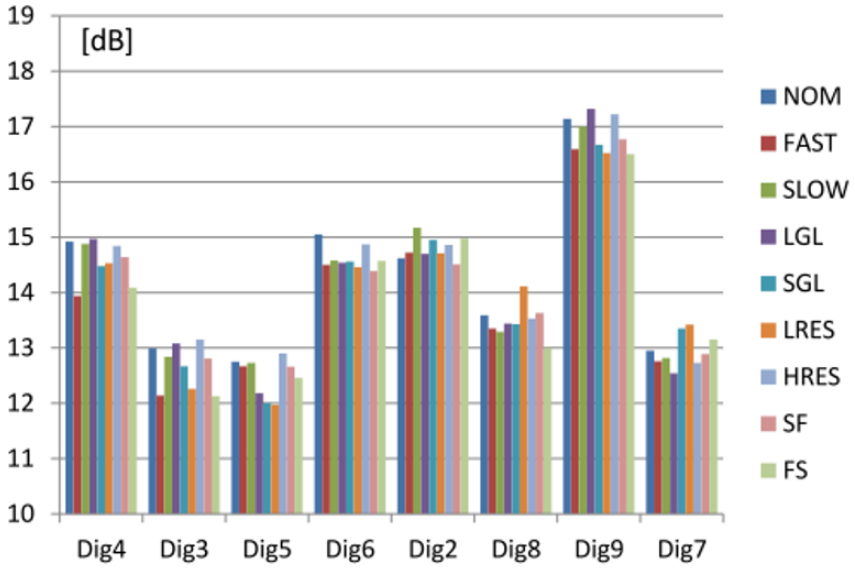


Victim → ΔΣ-DAC1 @ 50MHz Victim → ΔΣ-DAC5 @ 50MHz
Criteria → parasitic coupling of digital signals into analog output signal
→ Spectrum analyzer @ analog AIF output

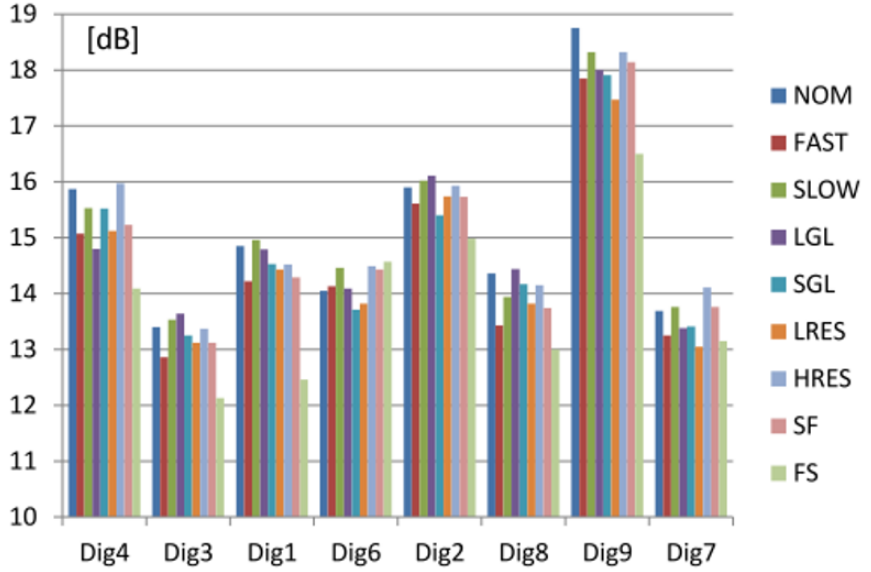
Aggressor → 1 of the other DIG circuits @ 49.5 & 50.5 MHz clock

MEASUREMENT

Difference between 50 MHz coupling and interference at 49.5 MHz

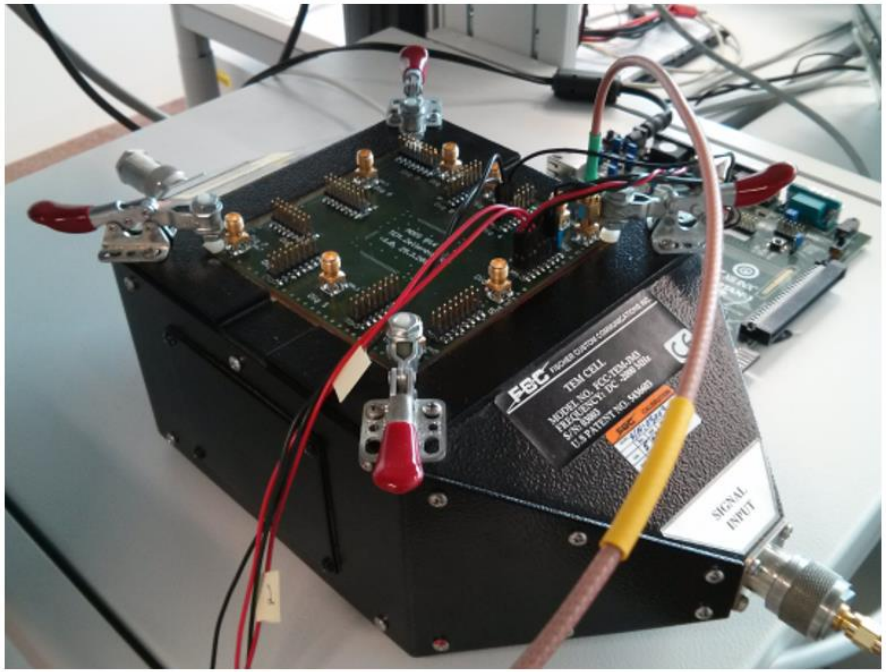


AIF output ΔΣ-DAC1

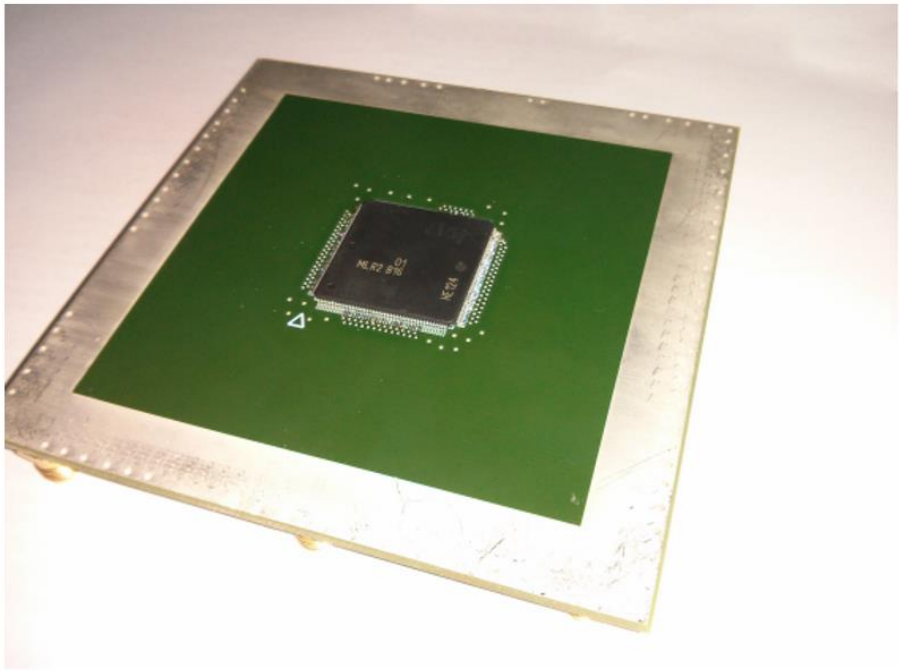


AIF output ΔΣ-DAC5

MEASUREMENT
→IEC 61967 TEM CELL EME MEASURMENT



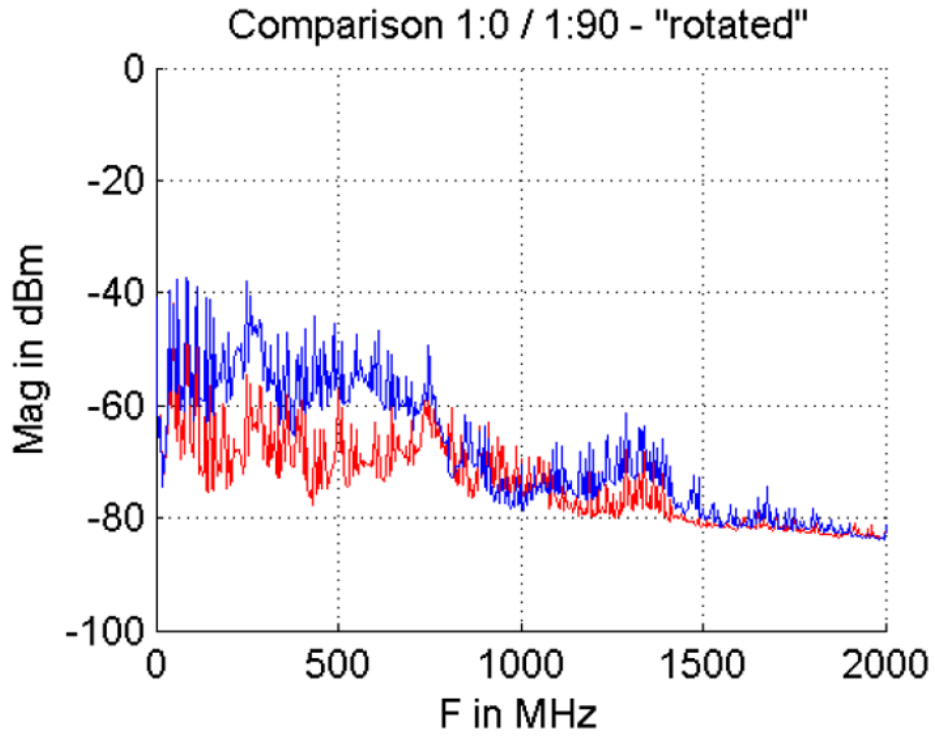
TEM cell with mounted test board



test board with DUT

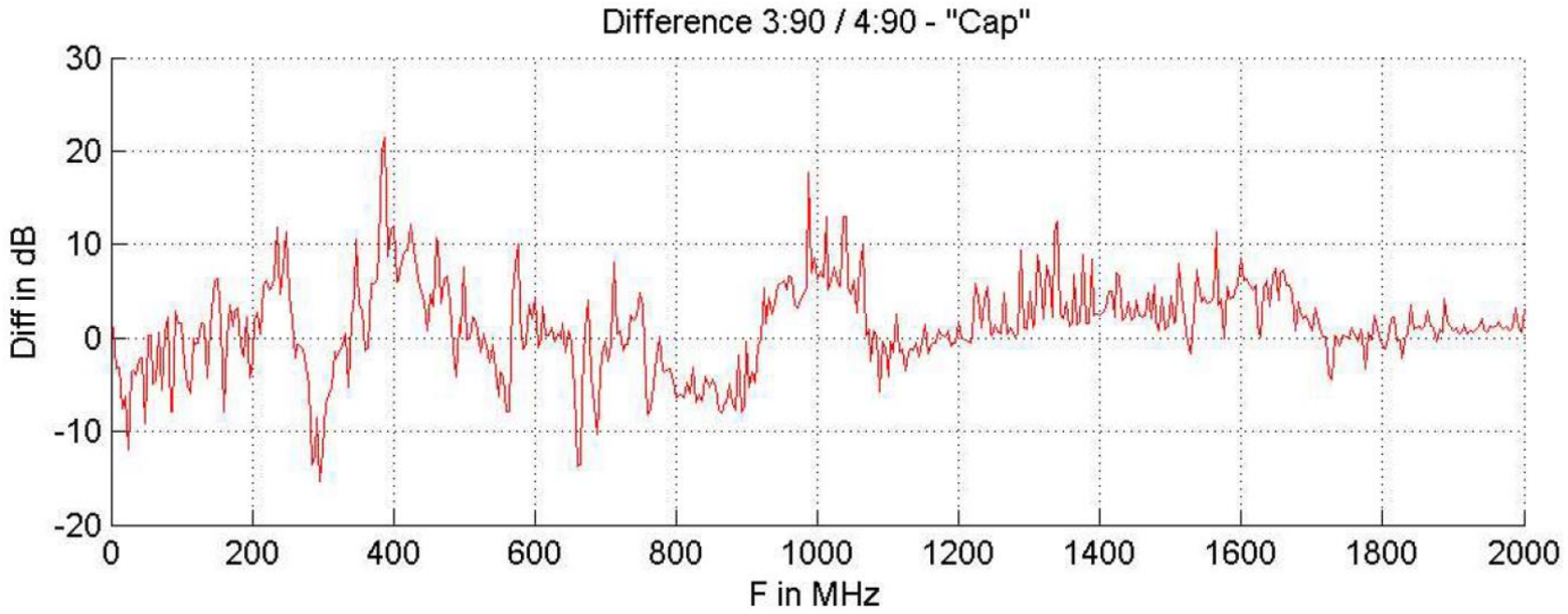
→ 1 50Ω TEM cell port is terminated with 50Ω load
→ 1 50Ω TEM-cell port is connected to the input of a spectrum analyzer
→ DUT is measured four times, each time rotated by 90°

MEASUREMENT
→IEC 61967 TEM CELL EME MEASURMENT



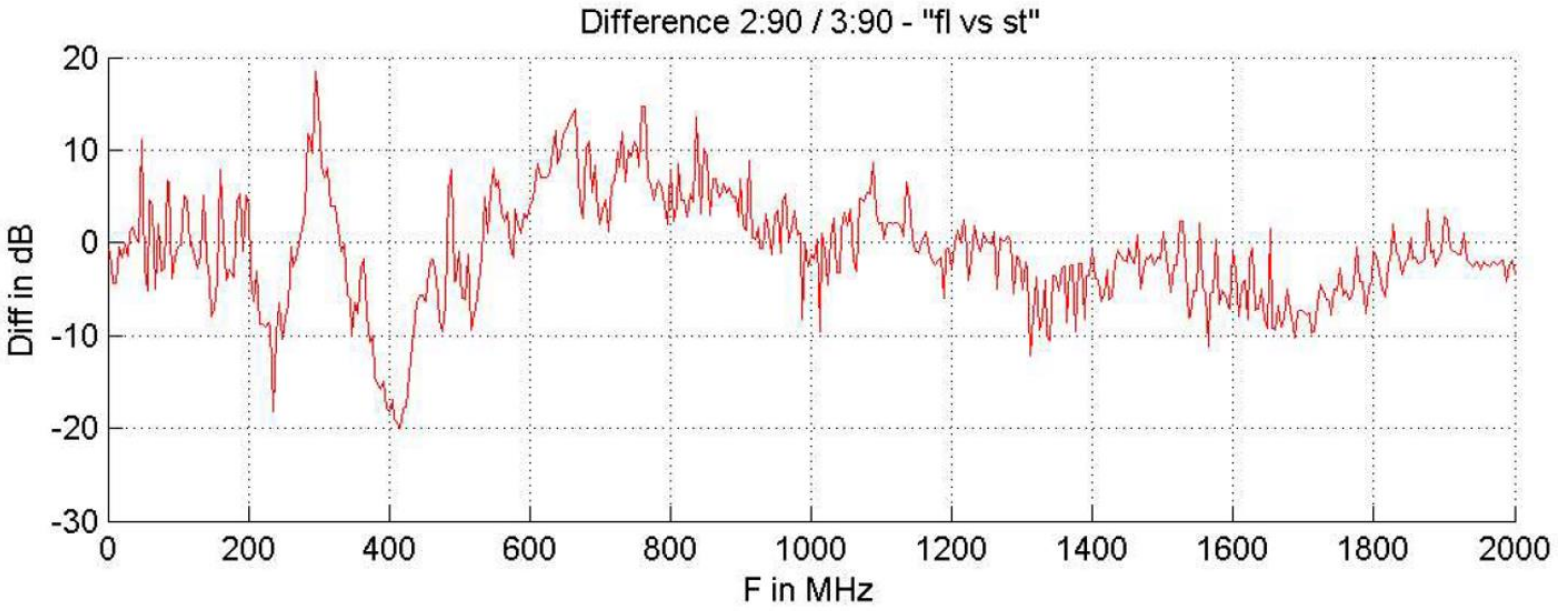
Measurement of ΔΣ-DAC1 (nominal corner)
@ 50MHz, [9 kHz - 2 GHz]

MEASUREMENT
→IEC 61967 TEM CELL EME MEASURMENT



Differences between the measured EME of
→ DIG3 (filler cells with capacitances)
→ DIG4 (filler cells without capacitances)

MEASUREMENT
→IEC 61967 TEM CELL EME MEASURMENT



Influence of the power ring layout between DIG2 (stacked) and DIG3 (flattened)

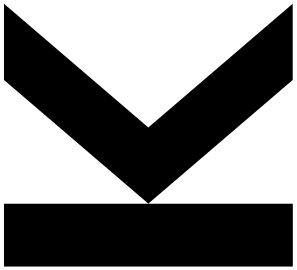
Again no improvement over the whole frequency range can be observed for neither variant.

CONCLUSION

- Overall recommendation:
  - Stacking the power rings to save space can be recommended, at least as long as no routing problems occur.
  - Stacking of the power rings result in no degradation considering emissions.
  - Considering emissions only, the use of filler cells with capacitances has no benefits. Although their use can be recommended as they reduce on chip interferences.

JOHANNES KEPLER
UNIVERSITY LINZ

THANK YOU!



JOHANNES KEPLER
UNIVERSITY LINZ
Altenberger Strasse 69
4040 Linz, Austria
www.jku.at