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SPI 2019

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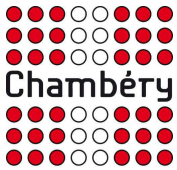
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Dear colleagues and friends,

This is the second time I have the honor of serving as Chair of the IEEE Workshop on Signal and Power Integrity (SPI). The 23rd edition of SPI will be hosted by the magnificent city of Chambéry in the French Alps. The event is organized by the IMEP–LAHC laboratory and the Lab-STICC under the patronage of the Université de Savoie Mont Blanc, the Université de Bretagne Occidentale and the Ecole Nationale d'Ingénieurs de Brest.

SPI stays true to its reputation as a leading international conference in the field of Signal and Power Integrity. We are expecting participants from three continents. The program features a balanced selection of topics ranging from modeling to characterization and includes a special session titled “Emerging Substrate-Integrated Technologies” chaired by Dr. Anthony Ghiotto. The SPI Industry Forum is also back with a new edition organized and chaired by Dr. Aida Todri-Sanial.

This year’s tutorial talks are exclusively dedicated to Si/Pi for automotive applications and are presented by engineers with first-hand experience of this emerging field – Yan Fen Shen and Ben Silva from the IoT Group, Intel Corporation and Stefanie Schatt from Continental Automotive.

We also have the privilege to welcome the co-founder of Kapteos, Dr. Gwenaël Gaborit who is this edition’s Keynote Speaker.

Social events were carefully organized in the long standing tradition of the workshop. Participants will be able to discover the historic city of Chambéry, taste the exquisite local cuisine and enjoy the magnificent scenery of the French Alps.

I must express my gratitude to SPI authors; their work is the foundation of this conference. I am also grateful to the sponsors; the event would not be possible without their contribution. I was fortunate to have a reliable organization committee and I thank all the colleagues involved. The SPI Standing Committee has, as always, provided precious guidance and the Technical Program Committee was instrumental in selecting the papers. I thank them for their work.

I wish everyone an enjoyable and successful event and good fortune to future SPI organizers!

Mihai Telescu

SPI2019 General Chair

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Tuesday June 18th

13:50 14:10 Tutorials Welcome

14:10 15:30 Tutorials

Power and Signal Integrity Challenges in IoT Automotive Applications

Yan Fen Shen (IoT Group, Intel Corporation), Ben Silva (IoT Group, Intel Corporation)

The emergence of connected smart vehicles has fully transformed the in-vehicle experience, connecting drivers and technology, and will revolutionize the future of mobility. In this tutorial, we will discuss the latest trend in IoT automotive applications and the associated SoC+platform Signal Integrity (SI) & Power Integrity (PI) design challenges. Based on the desired level of vehicle autonomy and criticality of specific design features, electronics in the vehicle are categorized into different classifications/grades (AEC, ASIL, etc.) relative to capabilities, limitations, and functional safety. The end product dictates the use conditions that the vehicle's electronics must adhere to, including manufacturing, testing, thermal, and reliability. These use conditions can be much more stringent than standard consumer products and require diligent SI/PI engineering to work around these design challenges. At the same time, SI and PI performance enablers are in direct opposition to one another, so it becomes necessary to balance both disciplines and view the total system holistically to provide the best possible system performance. Examples of SI/PI challenges, tradeoffs, compromises, and simulation results will be presented.

Yan Fen Shen *is a senior Power Integrity technical lead and project lead at Intel Corporation in the Internet of Things (IoT) Group. She has 17yrs of experience working in the field of Power Integrity, covering client computing and IoT products. Her interest and area of expertise are SoC+pl atform system level design and optimization, while pushing the envelopes of the latest technologies. She's also had firsthand experience working with end customers by conducting Power Integrity training classes, reviewing customer designs, and providing design guidelines. Her recent work includes autonomous, computer vision, FIVR, and LPDDR5 developments.*

Ben Silva *is the technical lead and manager of the signal and power integrity team within the Internet of Things Group at Intel. He has been working in the field of signal and power integrity for almost 20 years with his current focus being system level signal/power integrity optimization and design. His past work focused on package level power integrity optimization, HSIO channel modeling/margin estimation, and full channel DDR modeling. His other interests include creating new signal/power integrity flows/methodologies to accelerate the product development cycle and simulation to lab correlation.*

15:30 16:10 Coffee break

16:10 17:50 Tutorials

Autonomous driving as one of the key drivers for high speed design in automotive developments

Stefanie Schatt (Continental Automotive)

The development of advanced driver assistance systems especially for autonomously driving cars demands the integration of high speed interfaces to an extent previously unknown in automotive designs. The presentation will cover the specialties for signal and power integrity in today's automotive designs and give an overview over commonly used interfaces. One focus will also be the simulation sign-off of DDR4/LPDDR4/LPDDR4X interfaces which is specifically challenging due to the various constraints that are given by JEDEC, different vendors and technology.

Stefanie Schatt *is an expert for high speed design simulation at Continental (Germany) with a strong focus on automotive applications. She provides specialized technical support in the field of signal integrity, power integrity and IRdrop on PCB level as well as 3D EMC simulations; she is involved in the development of flows and strategies to sign off complex designs. Before joining Continental, she worked for companies such as Cadence Design Systems and Infineon Technologies. She has 20 years of experience and a strong international background having worked with US and French-based engineering teams.*

18:15 Special tour and Welcome reception

Wednesday June 19th

8:00 8:40 Welcome and Registration

8:40 9:20 Opening Session

9:20 10:20 Keynote speech

Optical sensing for the vectorial analysis of ultra-wideband electric field - requirements, performances and applications

Gwenaël Gaborit (Kapteos)

The electric (E) field analysis is of major importance, and even mandatory, for many academic or industrial topics, such as energy monitoring, high voltage device contactless diagnostics, near field antenna characterization, bioelectromagnetism, electromagnetic compatibility, human exposure, military defence… Nevertheless, the exhaustive E-field measurement can be very complex due to the environment (very confined, presence of high magnetic field, near field configuration), to its intrinsic properties (e.g. close to or over the disruptive value, exotic polarization state, ultra-short pulse) or to societal/economic constraints. This keynote is focused on electro-optical (EO) sensing probes leading to a non-invasive and vectorial characterization of the E-field in environments and conditions not suitable for classical antennas. All the relevant characteristics leading to a comprehensive E-field measurement will be firstly defined and the EO effect will be explained. Then, a comparison with other widespread techniques (classical metallic transducers, bolometer, optoelectronic antennas…) will clarify strengths and limitations of this optical technique. The core of the presentation is dedicated to the experimental assessment of the field with several examples associated to the above identified applications. Measurement from quasi-DC up to terahertz region will be presented and analysed, for fields in guided or radiated configuration. Environments such as air, biological media or plasma are considered. I will also discuss the validity and the accuracy of absolute E-field measurements, depending obviously on the probe itself but also, dramatically, on the calibration procedure.

Gwenaël Gaborit *was born in Lens, France, in 1978. He received the M.Sc. degree in Microwaves and Microelectronics from the University of Lille, France, in 2002. He received the Ph.D. Degree in Physics from the University of Savoie, France, in 2005. In 2005 he joined IMEP-LAHC laboratory as an associate professor. In 2009 he co-founded Kapteos and has been the company's Chief Science Officer ever since. He obtained his HDR (Habilitation à Diriger des Recherches) from the University Savoie-Mont-Blanc in 2014. His main research interests concern the development of electro-optic sensors dedicated to non-invasive electric field measurement. He is also involved in THz generation, detection and propagation.*

Sponsor exhibition opens

10:20 10:50 Poster exhibition / Coffee break

10:50 12:10 Session 1 - Modeling and Design Flow for SI/PI *(Chair: P. Manfredi)*

10:50 - Performance Metrics for Crosstalk on Printed Circuit Boards in Frequency Domain - K. Scharff, H.-D. Bruns and C. Schuster - Institute of Electromagnetic Theory, Hamburg University of Technology, Hamburg, Germany

11:10 - Prediction of Frequency Dependent Shielding Behavior for Ground Via Fences in Printed Circuit Boards – T. Hillebrecht, D. Dahl and C. Schuster - Institute of Electromagnetic Theory, Hamburg University of Technology (TUHH), Hamburg, Germany

11:30 - Package Design Methodology for Crosstalk Mitigation between DC/DC Converter and ADC Analog Inputs in Complex SoC - F. Settino[1,2], T. Brandtner[1], J. Nieder[1], F. Praemassing[1], H. Koffler[1], P. Palestri[3], F. Crupi[2] - [1]Infineon Technologies Austria; [2]DIMES, University of Calabria, Italy; [3]DPIA, University of Udine, Italy

11:50 - A Novel Programmable Delay Line for VLSI Systems - A. Bal[1], J.N. Tiwari[1], J.N. Tripathi[1], R. Achar[2] - [1]STMicroelectronics, Greater Noida, India; [2]Carleton University, Ottawa, Canada

12:10 13:30 Lunch break

13:30 13:50 Special session introduction

13:50 15:30 Session 2 (Special) - Emerging Substrate Integrated Technology
(Chair: A. Ghiotto)

13:50 - A Review of Compact Substrate Integrated Waveguide (SIW) Interconnects and Components - M. Bozzi[1], L. Perregrini[1] and C. Tomassoni[2] - [1]Dept. of Electrical, Computer and Biomedical Engineering, University of Pavia, Italy; [2]Department of Engineering, University of Perugia, Italy

14:10 - Low Loss SISL Patch-Based Coupler with Arbitrary Coupling Coefficient - Y. Wang[1] and K. Ma[2] - [1]School of Physics, University of Electronic Science and Technology of China, Chengdu; [2]School of Microelectronics, Tianjin University, China

14:30 - Passive Opto-Antenna using Air-Filled Substrate-Integrated-Waveguide Technology – O. Caytan[1], L. Bogaert[1,2], H. Li[1], J. Van Kerrebrouck[1], S. Lemey[1], J. Bauwelinck[1], P. Demeester[1], G. Torfs[1], D. Vande Ginste[1] and H. Rogier[1] – [1]IDLab, Department of Information Technology, Ghent University; [2]Photonics Research Group, Department of Information Technology, Ghent University/imec

14:50 - Use of Multilayered-PCB for Q-band Substrate Integrated Waveguide Components – A. El Mostrah[1], A. Manchec[1], Y. Clavet[1], and M. Cariou[2], M. Sanchez-Soriano[2], C. Quendo[2], B. Potelon[2] - [1]Elliptika, Brest, France; [2]Univ Brest, Lab-STICC, CNRS, UMR 6285, Brest, France

15:10 - Recent Advances in Filter Design Using The AFSIW Technological Platform - T. Martin[1,2,3], A. Ghiotto[1] and T.-P. Vuong[3] - [1]IMS, Univ. Bordeaux, France ; [2]Cobham Microwave, Cobham plc, Gradignan, France ; [3]IMEP-LAHC, Grenoble, France

15:30 16:10 Session 3 - Stochastic / Sensitivity Analysis *(Chair: D. Vande Ginste)*

15:30 - A Hierarchical Approach to the Stochastic Analysis of Transmission Lines via Polynomial Chaos - P. Manfredi and R. Trinchero - Department of Electronics and Telecommunications, Politecnico di Torino, Italy

15:50 - Statistical Analysis of the Efficiency of an Integrated Voltage Regulator by means of a Machine Learning Model Coupled with Kriging Regression - R. Trinchero[1], M. Larbi[2], M. Swaminathan[2] and F. G. Canavero[1] - [1]EMC Group, Department of Electronics and Telecommunications, Politecnico di Torino, Italy; [2]School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, USA

16:10 17:50 Poster Session (includes Coffee break) *(Chair: O. Bayet)*

P1 CMOS Integrated PFM DC-DC Converter with Digitally-Controlled Frequency Selector - Junho Yu, Seungki Jeon, Hoyong Choi, and Namsoo Kim – School of ECE, Chungbuk National University, Cheong-ju, Korea

P2 An Energy Efficient Spectrum Shaping Scheme for Substrate Integrated Waveguides - Yu Zhao, R. Grünheid, G. Bauch – Institute of Communications, Hamburg University of Technology, Germany

P3 Via Transition Optimization Using a Domain Decomposition Approach – A. Carmona-Cruz[1], K. Scharff[2], J. Cedeño-Chaves[1], H-D. Brüns[2], R. Rimolo-Donadio[1] and C. Schuster[2] - [1]Department of Electronics Engineering, Instituto Tecnologico de Costa Rica (ITCR), Cartago, Costa Rica; [2]Institut fur Theoretische Elektrotechnik, Technische Universitat, Hamburg-Harburg, Germany

P4 Transmission Line Design for Testing High-Speed Integrated Circuits with Differential Signals – N. Bharat Thaker[1], R. Ashok[2], S. Manikandan[2], N. Nambath[3], S. Gupta[2] – [1]Silicon Photonics Product Division, Intel Technology India, Bengaluru, India; [2]Department of Electrical Engineering, IIT Bombay, Mumbay, India; [3]School of Electrical Sciences, IIT Goa, Ponda, India

P5 Frequency-Domain Characterization of Power Inductors for Class-E Resonant Converters – J. Bačmaga[1], R. Blečić[1], F. Pareschi [2,3], R. Rovatti [3,4], G. Setti [2,3], A. Barić[1] – [1]Department of Electronics and Telecommunications, Politecnico di Torino, Torino, Italy; [2]Advanced Research Center on Electronic Systems (ARCES), University of Bologna, Bologna, Italy; [3]Department of Electrical, Electronic and Information Engineering (DEI), University of Bologna, Bologna, Italy

P6 A Method to predict Radiated Susceptibility of Printed Circuit Board from Near-Field Scan Immunity - A. Boyer – LAAS-CNRS, Univ Toulouse, France

P7 Signal Quality Control for Cost-Effective Package Design - Jisoo Hwang, Heeseok Lee, Hoi-Jin Lee and Youngmin Shin – Design Technology Team, System LSI Division, Samsung Electonics, Hwaseong-si, Korea

P8 Modeling the Concentration Dependence for Manufacturing Single-Mode I/O Structures of MMI-Based Splitters in Thin Glass Sheets - J-P. Roth, T. Kühler and E. Griese – Theoretical Electrical Engineering and Photonics, University of Siegen, Germany

P9 Open Defect Detection of Through Silicon Vias for Structural Power Integrity Test of 3D-Ics – K. Hachiya[1], A. Kurokawa[2] - [1]Faculty of Modern Life, Teikyo Heisei University, Tokyo, Japan; [2]Graduate School of Science and Technology, Hirosaki University, Japan

P10 Power integrity Flow for mixed-signal NVM flash IP – X. Lecoq[1], A. Lipani[2] , S. Stemmer[1], A. Chimeno[3] - [1]STMicroelectronics Grenoble, MDG division, Grenoble, France; [2]STMicroelectronics Palermo, MDG division, Palermo, Italy; [3]STMicroelectronics Crolles, TR&D division, Crolles, France

18:15 Mountain and Lake Magic Tour

Thursday June 20th

8:00 8:40 Welcome and Registration

8:40 10:20 Session 4 - Macromodeling and Model Order Reduction
(Chair: S. Grivet-Talocia)

8:40 - On stabilization of parameterized macromodeling - A. Zanco, S. Grivet-Talocia, T. Bradde and M. De Stefano - Dept. Electronics and Telecommunications, Politecnico di Torino, Italy

9:00 - An IBIS-like Modelling for Power/Ground Noise Induced Jitter under Simultaneous Switching Outputs (SSO) - M. Souilem[1,4], J. N. Tripathi[2], W. Dghais[3,4,5] and H. Belgacem[3,4] - [1]Ecole Nationale d'Ingénieurs de Sousse, [3]Institut Supérieur des Sciences Appliquées et de Technologie, Université de Sousse, Tunisia; [2]STMicroelectronics Pvt. Ltd., Noida, India; [4]Laboratory of Elec. and Microelec. Université de Monastir, Tunisia; [5]Laboratoire d'Ingénierie des Systèmes Industriels et des Energies Renouvelables, ENSIT, Tunis

9:20 - A Bayesian Approach to Adaptive Frequency Sampling - S. De Ridder, D. Deschrijver, D. Spina, T. Dhaene and D. V. Ginste - IDLab, Department of Information Technology, Ghent University-imec, Belgium

9:40 - On the Extension of the TurboMOR-RC Reduction Method to RLC Circuits - F. Bekmambetova and P. Triverio - The Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Canada

10:00 - A Wide-Band Equivalent Circuit Model for Single Slot Defected Ground Structures - E. V. Nechel[1], F. Ferranti[2], Y. Rolain[1] and J. Lataire[1] – [1]Department of Fundamental Electricity and Instrumentation, Vrije Universiteit Brussel, Belgium; [2]Microwave Dept., IMT Atlantique, Lab-STICC, Brest, France

10:20 10:50 Poster exhibition / Coffee break

10:50 11:50 Session 5 - Electro-Magnetic Compatibility *(Chair: P. Xavier)*

10:50 - Finite element analysis of cable shields to investigate the behavior of the transfer impedance with respect to fast transients - S. Bauer[1], C. Türk[2], W. Renhart[1] and O. Bíró[1] - [1]Institute of Fundamentals and Theory in Electrical Engineering, Graz, Austria; [2]Ministry of Defence of Austria, Vienna, Austria

11:10 - Influence of Different Digital Power Supply Layout Styles on the EME of ICs with Respect to Process Variations - A. Rauchenecker and T. Ostermann - Dept. Energy Efficient Analog Circuits and Systems, Institute for Integrated Circuits, JKU University of Linz, Austria

11:30 - Study of the coupling of wide band Near Field Scan probe dedicated to the investigation of the radiated immunity of Printed Circuit Boards - A. Durier[1,2], S. Ben Dhia[2] and T. Dubois[3] – [1]MEA- CMR, IRT Saint Exupery, Toulouse, France; [2]ESE, LAAS-CNRS / INSA Toulouse, France; [3]IMS Bordeaux, France

11:50 12:30 Session 6 - Measurements and Characterization *(Chair: M. Le Roy)*

11:50 - A Method to Determine Wide Bandgap Power Devices Packaging Interconnections - L. Pace[1,2], N. Defrance[2], J-C. De Jaeger[2], A. Videt[1] and N. Idir[1] - [1]Laboratory of Electrical Engineering and Power Electronics; [2]IEMN, University of Lille, France

12:10 - Turnkey Methodology for Characteristic Impedance Extraction of Embedded Transmission Lines - G. Houzet, P. Artillan, C. Bermond, T. Lacrevaz and B. Flechet – IMEP-LaHC, University Savoie Mont-Blanc, Le Bourget du Lac, France

12:30 13:50 Lunch break

13:50 15:10 Session 7 - Interconnect Design and Optimization *(Chair: G. Houzet)*

13:50 - Mode Conversion Due To Residual Via Stubs in Differential Signaling - J. Cedeno-Chaves[1], K. Scharff[2], A. Carmona-Cruz[1], H.-D. Bruns[2], R. Rimolo-Donadio[1] and C. Schuster[2] – [1]Department of Electronics Engineering, ITCR, Cartago, Costa Rica; [2]Institut für Theoretische Elektrotechnik, TUHH, Hamburg, Germany.

14:10 - Thermal and Signal Integrity Analysis of Novel 3D Crossbar Resistive Random Access Memories - F. Zayer[1,2,3], K. Lahbacha[1], W. Dghais[1,3], H. Belgacem[1,3], M. de Magistris[4], A. V. Melnikovand[5], A. Maffucci[6,7] - [1]Laboratory of Elec. and Microelec., [2]National Eng. School of Monastir, Tunisia; [3]Higher Inst. of Applied Science and Technology of Sousse, University of Sousse, Tunisia; [4]Dep. Electrical Eng. & Inform. Techn. University of Naples Federico II, Italy; [5]Institute for Nuclear Problems, Belarusian State University, Minsk, Belarus; [6]Dept of Electrical and Information Engineering, Univ. of Cassino and Southern Lazio, Italy; [7]INFN, Institute for Nuclear Physics, Frascati, Italy

14:30 - Analysis of Jitter for a Chain-of-Inverters including On-chip Interconnects - M. Suhail Illikkal[1], J. N. Tripathi[2], H. Shrimali[1] and R. Achar[3] – [1]School of Computing and Electrical Engineering, Indian Institute of Technology Mandi, India; [2]ST Microelectronics, Greater Noida, India; [3]Carleton University, Ottawa, Canada

14:50 - Optimization of a Miniaturized Ethernet 10 Gbits/s 8 Conductors Interconnect for Harsh Environments - Y. Boujmad[1], P. Artillan[1], C. Bermond[1], O. Gavard[2], M. Prudhom[2], F. Khalili[2], E. Husson-Charlet[2], J.-P. Barbosa[2] and B. Flechet[1] - [1]IMEP-LaHC, Le Bourget du Lac, France; [2]Amphenol-Socapex, Thyez, France

15:10 15:50 Poster exhibition / Coffee break

15:50 17:50 Interactive Industry Forum

Invited Talks:

Trends and challenges of package electrical modeling in automotive context

Aurora Sanna (Back-End Manufacturing and Technology R&D, STMicroelectronics)

In the context of digital integrated circuits development, a growing focus on package electrical modeling is observed due to increasing operating frequencies, that make the impact of short interconnections potentially critical. In addition, package technology complexity is constantly evolving. Different platforms are available, each having its modeling challenges. Ball grid array (BGA) platform is now the standard for high-end automotive digital devices thanks to layout flexibility, that allows high interconnections density and multiple devices integration. Since many variables are involved, the electrical performance becomes strongly design-dependent and difficult to predict without accurate simulations. High density represents a challenge for simulation tools, that have to mesh very small details and provide accuracy combined to reasonable hardware requirements and runtime. A key aspect of package modeling is the strong link with design flow: simulation supports all the stages from pre-layout strategy definition to final post-layout validation. Following the trend to develop silicon, package and PCB in a co-design mode, a co-simulation approach is also needed: key aspects are tools automation, models standardization, data protection, parametric analysis. The automotive market has strict requirements in terms of electromagnetic emissions, leading to increasing interest in package-level shielding and decoupling techniques. The significant current density in advanced devices also puts the focus on electromigration effects and electro-thermal interaction, promoting a multiphysics approach.

Aurora Sanna *got the master's degree in Electronic Engineering at Politecnico di Milano in 2011. She started working on electrical simulations at PCB level, focusing on electromagnetic emissions and then moving to power and signal integrity. She progressively extended her experience from PCB level to system level, including package and die effects. In 2017 she joined the BGA package development team at STMicroelectronics, inside Back-End Manufacturing and Technology R&D organization based in Agrate Brianza, Italy. She is now in charge of package level and system level electrical modeling for package pre-layout and post-layout assessment. Her work is particularly focused on automotive products.*

3D-ADTCO: Architecture, Design and Technology Co-Optimization platform for High Energy Efficient 3D ICs

Sébastien Thuries - CEA-LETI

3D Technologies appear as a road to sidestep moore's law stagnation by providing high energy efficient vertical interconnect suitable interposer based computing system down to tight memory & logic integration . It is also suitable for heterogeneous compact integration required by smart sensors (AI). However, exploiting the third dimension raises many challenges in order to provide optimized 3D ICs, such as architecture partitioning, design methodology, technology reliability, while considering the cost of fabrication. In this talk, the speaker will present CEA-LETI's 3D architecture design and technology roadmap and associated co-optimization platform to optimize the power, performance,

area, and cost of M3D ICs. The speaker will introduce architecture breakthroughs possible thanks to High Density 3D (pitch < 1 µm) and an overview of specific 3D ICs silicon prototypes CEA-LETI is currently designing and fabricating. He will present the 3D design tool box with a special focus on the digital design methodology, including process design kit add-on for place and route within fabrication cost guidelines, as well as 3D ICs thermal, power and signal integrity verifications. An overview of the 3D technology at device level including last pure MOSFET device status and its performance at low temperatures (CoolCubeTM), will also be exposed.

Sébastien Thuries *is leading the High-Density 3D Architecture and Design group at CEA-LETI including fine pitch 3D Stacking as well as Monolithic 3D (M3D). He has worked on and led several Digital ASIC developments for a set of application like 4G Digital Base Band, Complex Imagers, System on Chip, Mixed Signal RF over the last decade…He has been a pioneer in FDSOI digital design and back biasing capability. He leads the research team on new architecture and design paradigm raised by M3D-IC in order to optimize the full system to technology fields. Sébastien Thuries has received his Master Degree in 2003 from Institut des Sciences de l'Ingénieur de Montpellier (Poly'tech Montpellier) and joined CEA/Leti in 2004 as research engineer.*

Panel discussion

Sponsor exhibition closes

18:15 Gala Dinner

Friday June 21st

8:00 9:00 Welcome and Registration

9:00 10:20 Session 8 - Power Distribution Networks *(Chair: M. Hashimoto)*

9:00 - Understanding NAND AC Timing Parameters and How to Accurately Implement them in SI Simulation - S. Mobin and P. Balachander - Western Digital Corporation, Milpitas, CA, USA

9:20 - Power Delivery Network Pre-Layout Design Planning and Analysis Through Automated Scripting - C. M. Smutzer, C. K. White, C. R. Haider, and B. K. Gilbert - Mayo Clinic, Special Purpose Processor Development Group (SPPDG), Rochester, MN USA

9:40 - A Frequency-Dependent Target Impedance Method Fulfilling Both Average and Dynamic Voltage Drop Constraints - J. Chen, M. Hashimoto - Dept. Information Systems Eng., Osaka University, Japan

10:00 - Expert System Synthesis for Evolutionary Decoupling Capacitor Optimization - D. N. De Araujo and J. Pingenot - Electronic Board Systems Division, Mentor, a Siemens Business, USA

10:20 10:50 Poster exhibition / Coffee break

10:50 11:50 Session 9 - Microwave and mmWave Solutions for SiP and SoC *(Chair: T. Lacrevaz)*

10:50 - RF line impedance optimization methodology in laminate technologies - T. Monnier[1], S. Danaie[2] and L. Schwartz[3] – [1]ADL – Silicon Packaging; FMT – [2]EWS Services; Grenoble, [3]BEMT R&D – Central Packaging, STMicroelectronics, Grenoble, France

11:10 - Propagation Channel in Silicon in the Sub-THz Band for MPSoCs - I. El Masri, T. Le Gouguec and P.-M. Martin - Univ Brest, Lab-STICC, Brest, France

11:30 - Compact Analog All-Pass Phase-Shifter in 65-nm CMOS for 24/28 GHz on-Chip- and in-Package Phased-Array Antenna - M. L. Carneiro[1], M. Le Roy[1], A. Pérennec[1], R. Lababidi[2], P. Ferrari[3] and V. Puyal[4,5] – [1]Univ Brest, Lab-STICC, Brest, France; [2]Ensta-Bretagne, Lab-STICC, Brest, France; [3]University of Grenoble Alpes, TIMA Laboratory, France; [4]University of Grenoble Alpes, Grenoble, France; [5]CEA, LETI, MINATEC campus, Grenoble, France

11:50 12:30 Closing session

Friday June 21st

22nd European IBIS Summit

12:50 **IBIS welcome reception, sign-in, refreshments**

13:10 **Welcome and Introductions (M. Schaeder, Zuken, Germany)**

13:20 IBIS Chair's Report
R. Wolff, Micron Technology, USA

13:35 Addressing Non-Ideal TX-FFE Behavior of High-Speed Drivers through Hierarchical Waveform Approximations
C. Siviero, R. Trinchero, S. Grivet-Talocia, I. Stievano, T. Bradde, Politecnico di Torino, Italy; M. Telescu, Université de Bretagne Occidentale, France

14:20 An Adaptive Algorithm for Fully Automated Extraction of Passive Parameterized Macromodels
A. Zanco, E. Fevola, S. Grivet-Talocia, T. Bradde, M. De Stefano, Politecnico di Torino, Italy

15:05 **Break, refreshments**

15:20 Introducing IBIS Version 7.0
M. Mirmak, Intel Corporation, USA

15:50 IBIS File Format Links
B. Ross, Teraspeed Labs, USA

16:20 **Open discussion**

16:35 **Closing remarks (M. Schaeder, Zuken, Germany)**

16:40 **End of meeting**

SOCIAL EVENTS

WELCOME RECEPTION - Tuesday June 18th

Welcome reception at the convention center "Le manège". A rich buffet was selected including local specialties.

Chambéry is not only a popular destination for mountaineers but also a city with a very rich history. A visit of the ducal castle in Chambéry is scheduled before the traditional Welcome Reception.

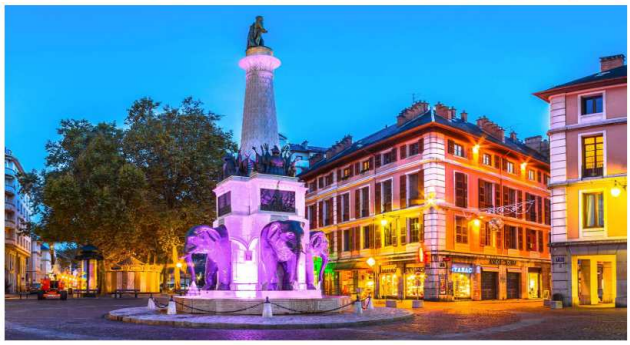
Mountain and Lake Magic Tour - Wednesday June 19th

Participants will have the opportunity to discover the Mountains near Chambéry and dine on the shores of the Bourget Lake.

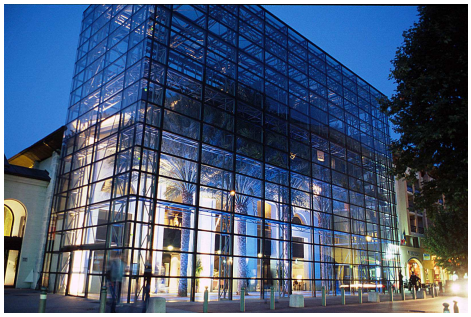
GALA DINNER - Thursday June 20th

The Gala Dinner will take place at the Domaines des Saints Pères where participants will discover the exquisite cuisine of the Savoy region and enjoy a magnificent view of the French Alps

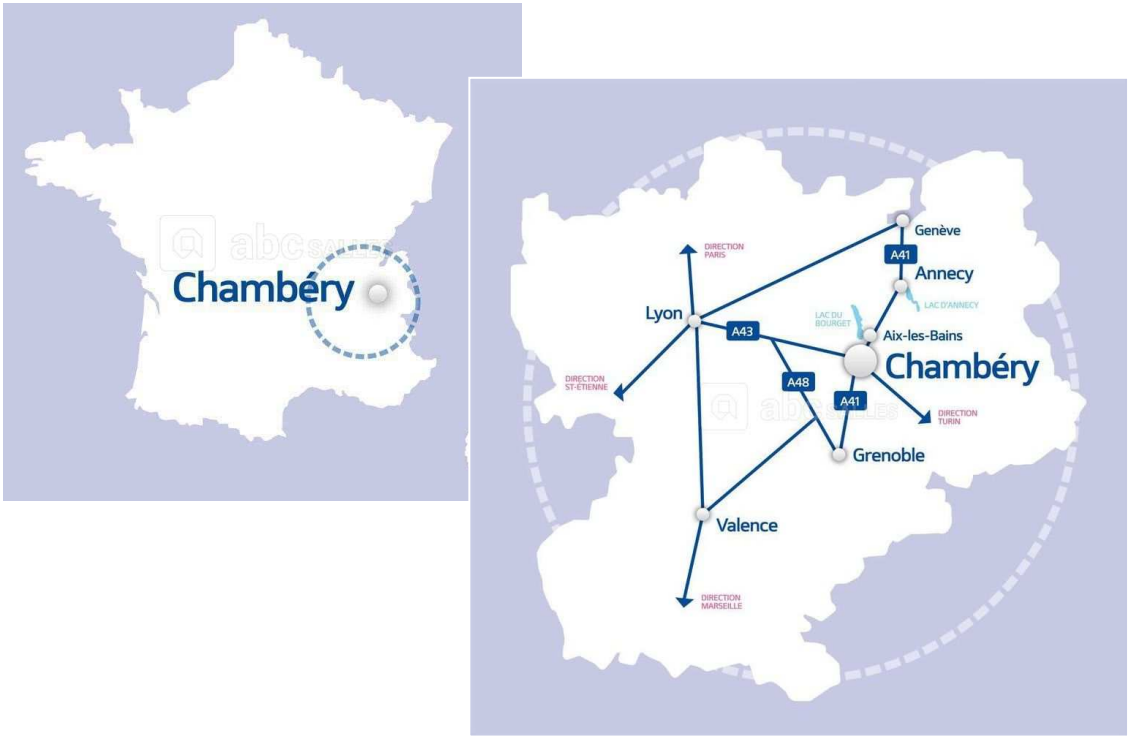





The 23rd IEEE Workshop on SPI will be hosted in the Convention Center "Le Manège", downtown Chambéry



Le Manège
331 Rue de la République,
73000 Chambéry, France



SPI 2019		Tuesday June 18th	Wednesday June 19th	Thursday June 20th	Friday June 21st	SPI 2019	
08:00	08:20		SPI 2019 Welcome and Registration	SPI 2019 Welcome and Registration	SPI 2019 Welcome and Registration	08:00	08:20
08:20	08:40					08:20	08:40
08:40	09:00		Openning Session	Session 4 Macromodeling and Model Order Reduction		08:40	09:00
09:00	09:20				Session 8 Power Distribution Networks	09:00	09:20
09:20	09:40		Keynote Optical sensing for the vectorial analysis of ultra-wideband electric field G. Gaborit (Kapteos)			09:20	09:40
09:40	10:00					09:40	10:00
10:00	10:20					10:00	10:20
10:20	10:50		Poster exhibition Coffee break	Poster exhibition Coffee break	Poster exhibition Coffee break	10:20	10:50
10:50	11:10		Session 1 Modeling and Design Flow for SI/PI	Session 5 Electro-Magnetic Compatibility	Session 9 Microwave and mmWave Solutions for SiP and SoC	10:50	11:10
11:10	11:30					11:10	11:30
11:30	11:50					11:30	11:50
11:50	12:10			Session 6 Measurements and Characterization	Closing Session	11:50	12:10
12:10	12:30		Lunch break			12:10	12:30
12:30	12:50			Lunch break		12:30	12:50
12:50	13:10				IBIS welcome Reception	12:50	13:10
13:10	13:30				IBIS European Summit	13:10	13:30
13:30	13:50		Special session introduction			13:30	13:50
13:50	14:10	Tutorials Welcome	Session 2 (Special) Emerging Substrate Integrated Technology	Session 7 Interconnect Design and Optimization		13:50	14:10
14:10	14:30	Tutorial Power and Signal Integrity Challenges in IoT Automotive Applications Yan Fen Shen & Benjamin Silva (Intel)				14:10	14:30
14:30	14:50					14:30	14:50
14:50	15:10					14:50	15:10
15:10	15:30			Poster exhibition Coffee break		15:10	15:30
15:30	15:50	Coffee break	Session 3 Stochastic / Sensitivity Analysis			15:30	15:50
15:50	16:10			Interactive Industry Forum		15:50	16:10
16:10	16:30	Tutorial Autonomous driving as one of the key drivers for high speed design in automotive developments Stefanie Schatt (Contiental)	Poster Session (includes Coffee break)			16:10	16:30
16:30	16:50					16:30	16:50
16:50	17:10					16:50	17:10
17:10	17:30					17:10	17:30
17:30	17:50					17:30	17:50

SPI 2019 From 17: 00,Welcome and Registration	Social entertainment	Social entertainment
18:15 - 22:00 Special Tour and Welcome reception	18:15 - 21:30 Mountain and Lake Magic Tour	18:15 - 23:30 Social Event