Power Delivery Network Pre-Layout Design Planning and Analysis Through Automated Scripting

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Agenda

- Contextual background on High Performance Compute (HPC) systems
- Motivation for pre-layout, automated Power Delivery Network (PDN) analysis in Printed Circuit Boards (PCB)
  - Process overview: File-driven inputs/outputs, tool integration
- Example 1: Simplified PCB pre-layout with broadband impedance Z(f) sensitivity
  - Sample decoupling capacitor quantity and location
- Example 2: First-level package pre-layout with DCIR current density analysis
  - Lumped vs. distributed loading
- Concluding remarks with additional practical applications

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Background – High Performance Compute Systems

- Several high-power processing nodes (often > 500 W each) systematically arranged using high-speed interconnect (~56 Gbps) to solve complex computational problems
  - Components often include: processors/FPGAs, memory, voltage regulation, passives, cooling and packaging
- Performance and capability can be limited by poor signal- and/or power-integrity design
  - Signaling rate dependent upon passive channel quality
  - Voltage noise dependent upon power distribution design
- Mayo Clinic SPPDG's role
  - Quick-turn, complex analyses, cost/schedule-aware, risk-based technical trade-space studies, etc.
  - Stay ahead of critical design path

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Motivation – Pre Layout PDN Analysis (1)

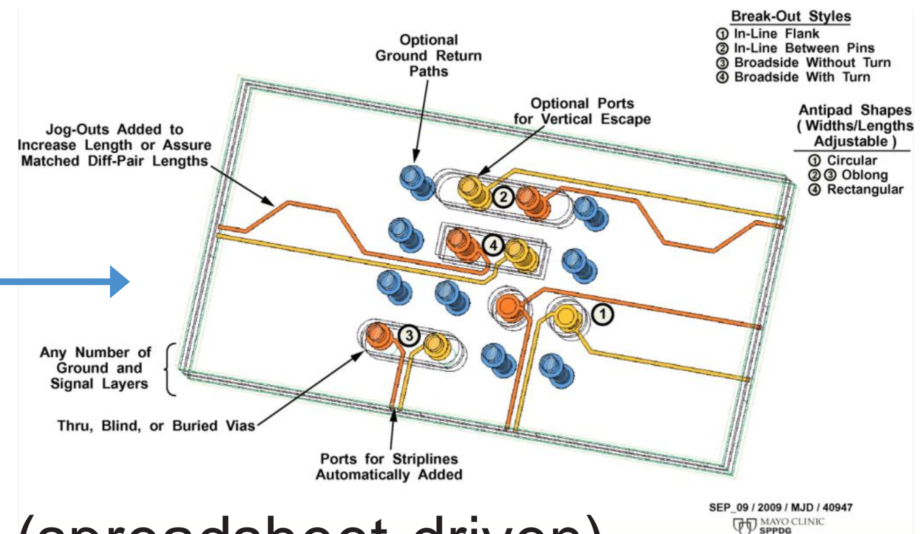
- Typical or common PDN design flow is _*Reactive*_
  - Stackup construction based largely on signaling needs; number of layers, location of power planes, materials, etc.
  - Rules-of-thumb often used for decoupling capacitor selection and placement
  - Post-layout PDN impedance extraction with comparison to Target Impedance requirements
    - If power delivery goals are unmet, may require significant CAD layout iteration(s) impacting many critical design features (component placement, stackup and materials, layer net allocations, signal routing, etc.)
  - Frequently results in over- or under-engineered PDN with consequences to schedule and cost

Motivation – Pre Layout PDN Analysis (2)

- Proposed PDN design flow is *Proactive*
  - Fast, efficient process to evaluate vast trade-space of power delivery design concepts prior to formal CAD implementation
    - Educational "what if" scenarios
    - Automation to create geometries (planes/shapes), place thousands of vias and decoupling capacitors, active devices, interfering connectors/breakouts etc.
    - Exploit seldom used feature in PDN simulation tools – scripting to generate these structures and analysis setups
  - Process results optimize packaging resources to provide sufficient power delivery performance while considering signal integrity – SI/PI co-design

Process Overview – Pre Layout PDN Analysis

- SI engineers model and optimize high-speed signal channels and pinfield breakouts (“PinBuilder”)



- Similar process proposed for PDN structure evaluation
- Generate visual design inputs (spreadsheet-driven)
- Execute processing script
  - Create 3D structures in field solvers based on input files
  - Apply supporting elements (ports, sources/loads, setup, etc.)
- Perform traditional PDN extractions (broadband impedance extraction, current density, etc.)
- Modify design inputs and iterate processing script

POWER DELIVERY NETWORK PRE-LAYOUT PLANNING AND ANALYSIS AUTOMATED SCRIPTING PROCESS

INPUTS

Via Padstacks

Via_Name	BB_L1_L2	
#Layer	Pad	Anti-Pad
1	0.032	0.036
(drill)	0.02	
2	0.032	0.036
(drill)	0.02	
3	0.032	0.036
(drill)	0.02	
4	0.032	0.036
Via_End		

Stackup, Materials, Layer Usage

Package Pinouts

Fabricator Design Rules

- Pad Pitch
- Aspect Ratio
- Min. Drill
- Stacked Vias
- Plating Thickness
- Via Plating
- Internal Pad Size
- Min. Metal Gap

SIMULATION RESULTS

Broadband Impedance Plots

freq=38.02MHz

Current Density Plots

OUTPUTS

PCB Layouts

Package Layouts

PROCESSING SCRIPT

```
'Add GND VRM pad and stitch vias
obj.ScrDrawRectangle brd_x-14.6, 25, brd_x-5, 50, "L1", "GND", "mm"
for n=1 to 25 step 1
obj.ScrDrawVia brd_x-14.6+pitch/2, 25+pitch/2+(n-1)*pitch, "L1", "L10", "V203L1-10_SE_A", "GND", 0, 0, 0, "mm"
obj.ScrDrawVia brd_x-14.6+3*pitch/2, 25+pitch/2+(n-1)*pitch, "L1", "L10", "V203L1-10_SE_A", "GND", 0, 0, 0, "mm"
obj.ScrDrawVia brd_x-5-pitch/2, 25+pitch/2+(n-1)*pitch, "L1", "L10", "V203L1-10_SE_A", "GND", 0, 0, 0, "mm"
obj.ScrDrawVia brd_x-5-3*pitch/2, 25+pitch/2+(n-1)*pitch, "L1", "L10", "V203L1-10_SE_A", "GND", 0, 0, 0, "mm"
next 'next n


'Add SIG pins for switching node of VRM phases and a single via to satisfy SIWave
obj.ScrDrawVia brd_x-9.8, 30, "L1", "L1", "PVRM_L1_A", "SIG", 0, 0, 0, "mm"
obj.ScrDrawVia brd_x-9.8, 30, "L1", "L10", "V203L1-10_SE_A", "SIG", 0, 0, 0, "mm"
obj.ScrDrawVia brd_x-9.8, 35, "L1", "L1", "PVRM_L1_A", "SIG", 0, 0, 0, "mm"
obj.ScrDrawVia brd_x-9.8, 35, "L1", "L10", "V203L1-10_SE_A", "SIG", 0, 0, 0, "mm"
obj.ScrDrawVia brd_x-9.8, 40, "L1", "L1", "PVRM_L1_A", "SIG", 0, 0, 0, "mm"
obj.ScrDrawVia brd_x-9.8, 40, "L1", "L10", "V203L1-10_SE_A", "SIG", 0, 0, 0, "mm"
obj.ScrDrawVia brd_x-9.8, 45, "L1", "L1", "PVRM_L1_A", "SIG", 0, 0, 0, "mm"
obj.ScrDrawVia brd_x-9.8, 45, "L1", "L10", "V203L1-10_SE_A", "SIG", 0, 0, 0, "mm"

'Add PWR VRM pads and stitch vias
obj.ScrDrawVia brd_x-19.4, 30, "L1", "L1", "PVRM_L1_A", "PWR", 0, 0, 0, "mm"
obj.ScrDrawVia brd_x-19.4, 35, "L1", "L1", "PVRM_L1_A", "PWR", 0, 0, 0, "mm"
obj.ScrDrawVia brd_x-19.4, 40, "L1", "L1", "PVRM_L1_A", "PWR", 0, 0, 0, "mm"
obj.ScrDrawVia brd_x-19.4, 45, "L1", "L1", "PVRM_L1_A", "PWR", 0, 0, 0, "mm"

for m=1 to 3
    for n=1 to 4 step 1
        obj.ScrDrawVia brd_x-19.4-(n-2.5)*pitch, 30+(m-2)*pitch, "L1", "L10", "V203L1-10_SE_A", "PWR", 0, 0, 0, "mm"
        obj.ScrDrawVia brd_x-19.4-(n-2.5)*pitch, 35+(m-2)*pitch, "L1", "L10", "V203L1-10_SE_A", "PWR", 0, 0, 0, "mm"
        obj.ScrDrawVia brd_x-19.4-(n-2.5)*pitch, 40+(m-2)*pitch, "L1", "L10", "V203L1-10_SE_A", "PWR", 0, 0, 0, "mm"
        obj.ScrDrawVia brd_x-19.4-(n-2.5)*pitch, 45+(m-2)*pitch, "L1", "L10", "V203L1-10_SE_A", "PWR", 0, 0, 0, "mm"
    next 'next n
next 'next m
```

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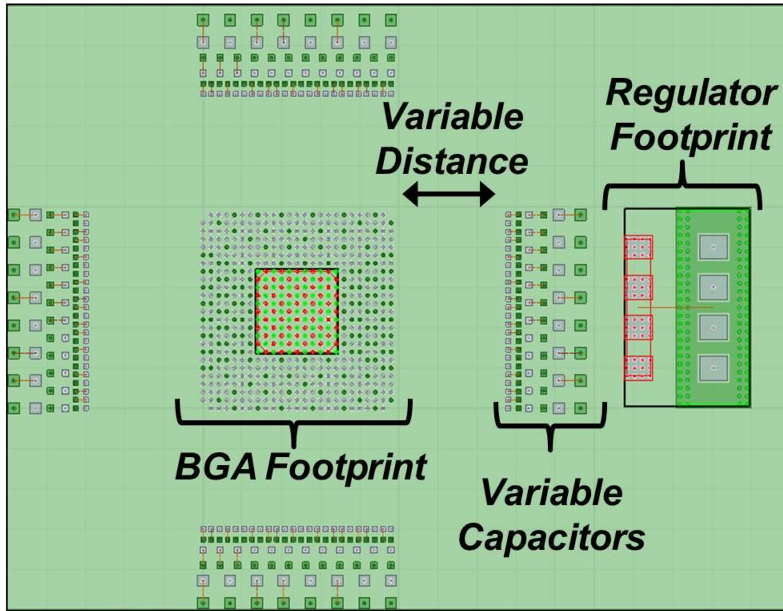
Example 1 – PCB PDN: Capacitor Sensitivity (1)

- Typical question: How can we influence PDN impedance with top-side discrete capacitors?
- Simplistic example (process demonstration focused) to study impact of PCB capacitor quantity and placement location on broadband PDN impedance
  - Representative of typical processor card in HPC system
  - Varying quantity of 3 capacitor sizes (1206, 0805, 0402) distributed around BGA footprint
  - Include provisions (layers, pinfield voids, etc.) for signaling
- All dimensions and locations specified in external input files
  - Excel files (visual) for via padstacks, VRM footprint, BGA pinout, PCB construction, layer assignments
  - Text-based file for other geometries, PCB design rules

POWER DELIVERY NETWORK DESIGN AUTOMATION - PRINTED CIRCUIT BOARD LAYOUT EXAMPLE

(a) PCB – TOP VIEW

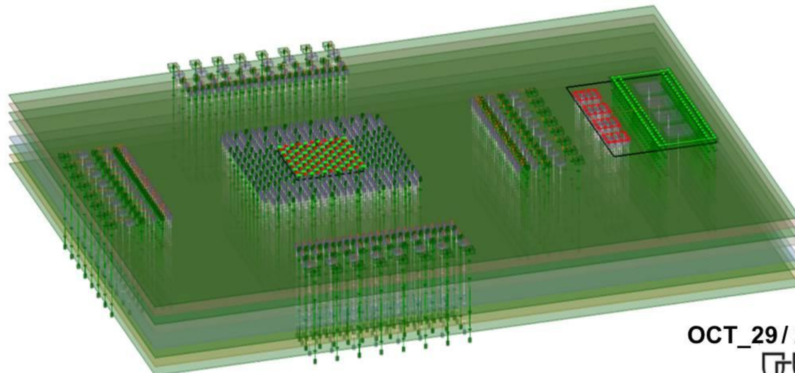


- 25 x 25 mm BGA footprint
- 1 mm BGA pitch
- 60 BGA for power in center region

(b) STACKUP

Lamination					Drills	Layer Usage	
Layer #	Dielectric	Copper Thickness (mil)	Dielectric Thickness (mil)	Visual		Version A	Version B
	Green		1.5				
1	Plated copper	2.60			8 mil Through-Hole	Attach	Attach
	FR4_epoxy		5				
2	copper	0.60				GND	GND
	FR-4		5				
3	copper	0.60				SIG	**PWR**
	FR4_epoxy		5				
4	copper	0.60				GND	GND
	FR-4		5				
5	copper	0.60				**PWR**	SIG
	FR4_epoxy		9				
6	copper	0.60				**PWR**	SIG
	FR-4		5				
7	copper	0.60				GND	GND
	FR4_epoxy		5				
8	copper	0.60				SIG	**PWR**
	FR-4		5				
9	copper	0.60				GND	GND
	FR4_epoxy		5				
10	Plated copper	2.60				Attach	Attach
	Green		1.5				

(c) PCB – 3D VIEW



(d) PCB VIA DESIGN

L1 to L10

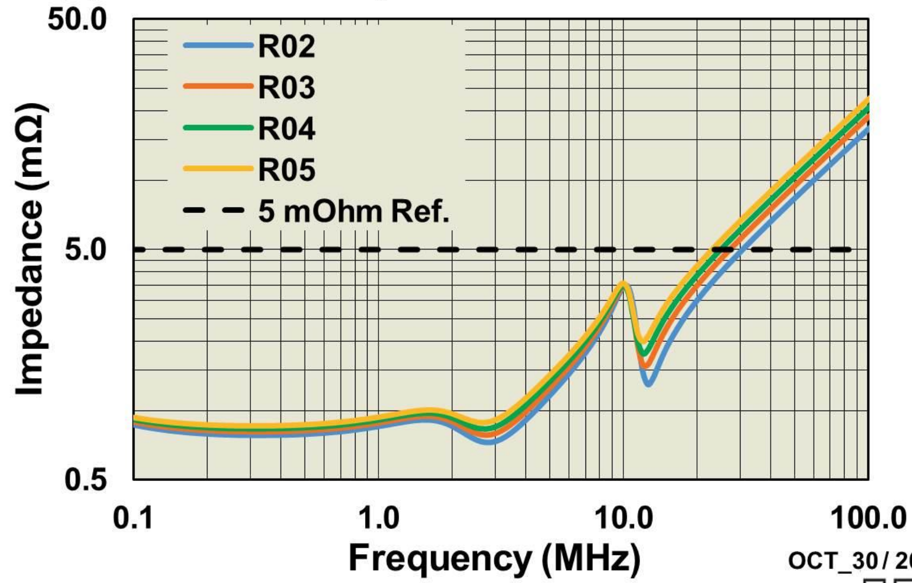
Name:	V203L1-10_SE_A
Drill Type:	Plated Thru Hole
Drill Diameter:	0.203 (8 mil)
Inner Pad Diameter:	0.457 (18 mil)
Top Pad Diameter:	0.254 (10 mil)
Bottom Pad Diameter:	NA
Antipad Style:	Circle
Antipad Diameter:	0.635 (25 mil)

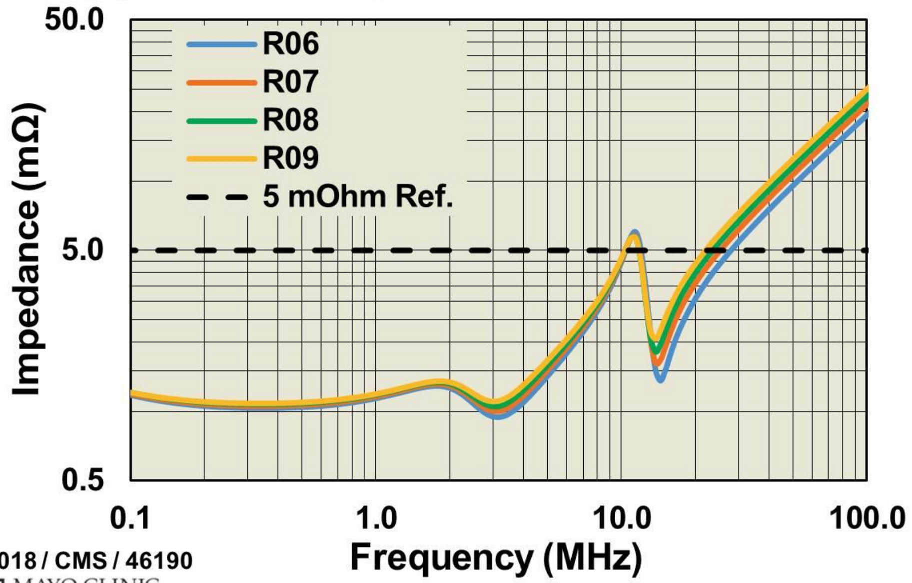
Example 1 – PCB PDN: Capacitor Sensitivity (2)

- Twelve configurations controlled through variables within the processing script
  - 4 distances
  - 3 capacitor quantities
- One additional configuration (layer net assignment) controlled through PCB construction spreadsheet
- Applied simulation ports to VDD/GND nets at BGA and VRM
- Extract broadband Z(f)

	Capacitor	Number of Capacitors		
Configuration	**Distance (mm)**	**0402**	**0805**	**1206**
Stackup Version A *(Power Layers in Center of Stack)*				
R02: Max. Caps, 2mm	2	96	48	32
R03: Max. Caps, 6mm	6	96	48	32
R04: Max. Caps, 10mm	10	96	48	32
R05: Max. Caps, 15mm	15	96	48	32
R06: Med. Caps, 2mm	2	48	24	16
R07: Med. Caps, 6mm	6	48	24	16
R08: Med. Caps, 10mm	10	48	24	16
R09: Med. Caps, 15mm	15	48	24	16
R10: Min. Caps, 2mm	2	24	12	8
R11: Min. Caps, 6mm	6	24	12	8
R12: Min. Caps, 10mm	10	24	12	8
R13: Min. Caps, 15mm	15	24	12	8
Stackup Version B *(Power Layers in Outer Portion of Stack)*				
R14: Min. Caps, 2mm	2	24	12	8

POWER DELIVERY NETWORK DESIGN AUTOMATION - PRINTED CIRCUIT BOARD BROADBAND IMPEDANCE PLOTS





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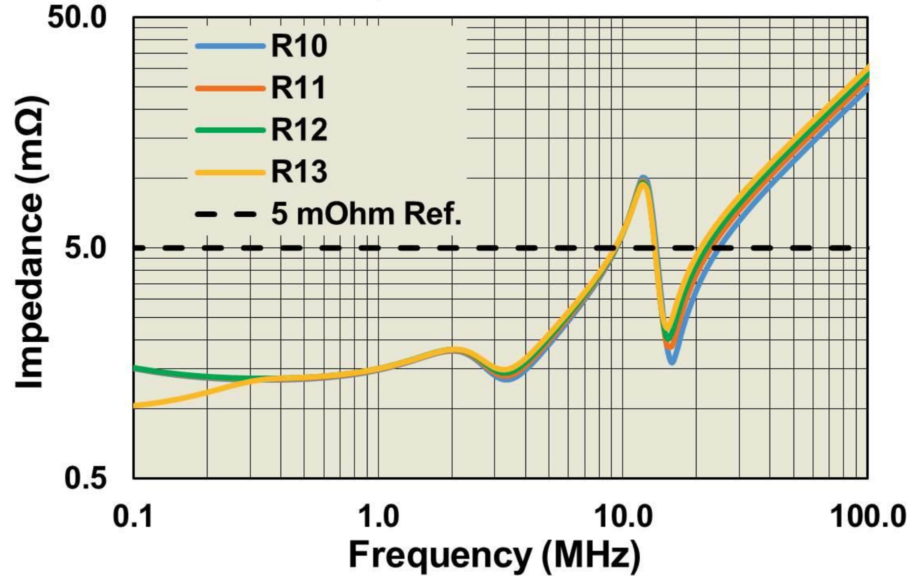

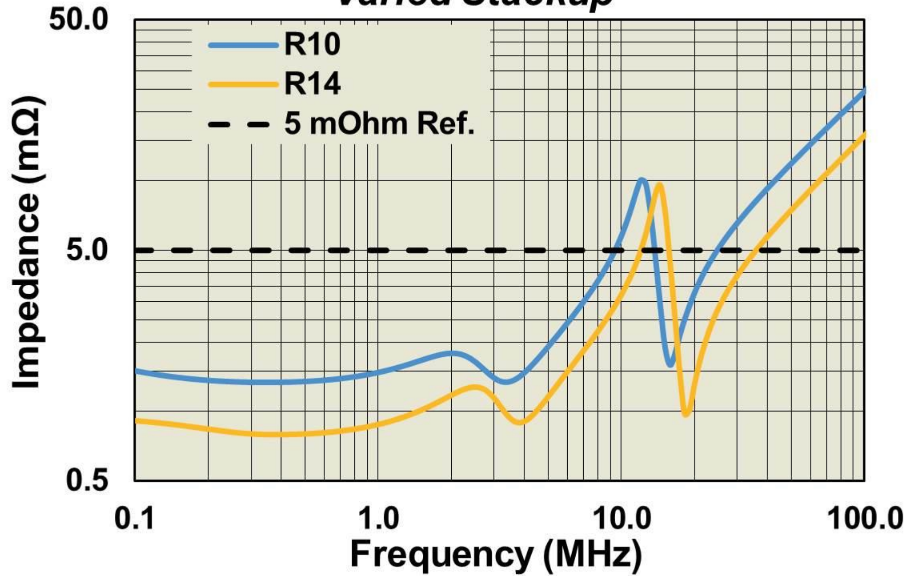

Example 1 – PCB PDN: Capacitor Sensitivity (3)

- Summary from 12 configurations of distance and quantity
  - Given the assumed PCB construction and layout, capacitor quantity had a greater impact on reducing PDN impedance than did the placement location
  - For each fixed number of capacitors, the placement location had very little influence on the impedance
- PCB capacitor loop inductance = mounted inductance + lateral (spreading) inductance + equivalent series inductance (ESL)
  - Speculated that via mounting inductance was dominant; hence, the effect of location was not being observed
  - Modified layer assignments (Version B) to reduce mounted inductance – observed appreciable impedance reduction for 2mm capacitor placement configuration

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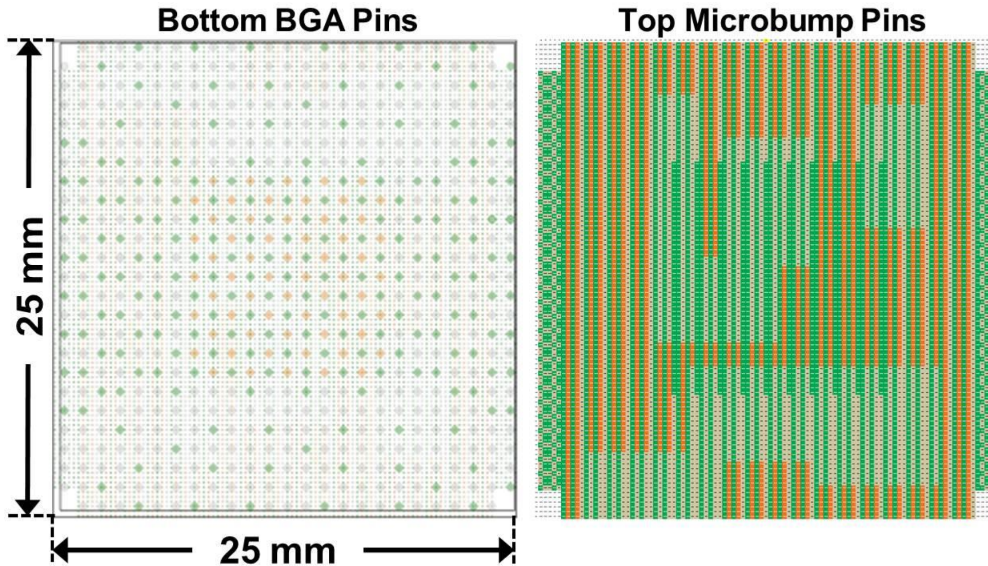
Example 2 – First Level Package: PDN DCIR (1)

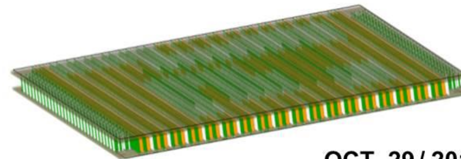
- Typical question: How can we strategically/proactively address current constriction and IR loss in micro-geometry designs?
- Simplistic example creates complex micro-geometry device package and analyzes using distributed and lumped loads
  - Represents typical first-level package for high-power IC
  - BGA interface on bottom, micro-bump interface on top
  - Include provisions (layers, pins, etc.) for signaling
- All dimensions and locations specified in external input files
  - Excel files (visual) for via padstacks, pinouts, construction
  - Text-based file for other geometries, fabricator design rules, distributed (per bump) current loads
  - Script created 3D package with massive quantity of build-up vias and tiny geometries in minutes

POWER DELIVERY NETWORK DESIGN AUTOMATION - FIRST-LEVEL PACKAGE LAYOUT EXAMPLE

(a) Package Design



- 1 mm BGA pitch
- 250 um microbump pitch
- 60 BGA for power
- 2247 microbumps for power



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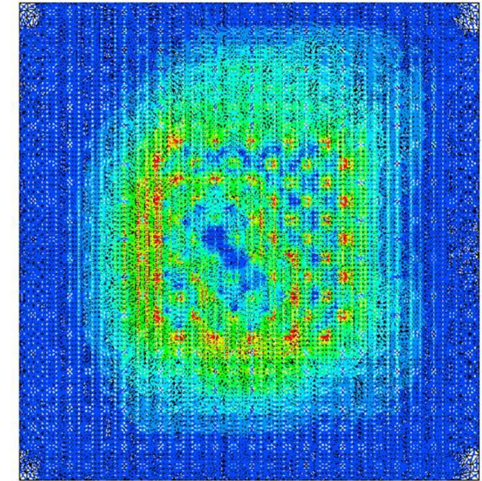
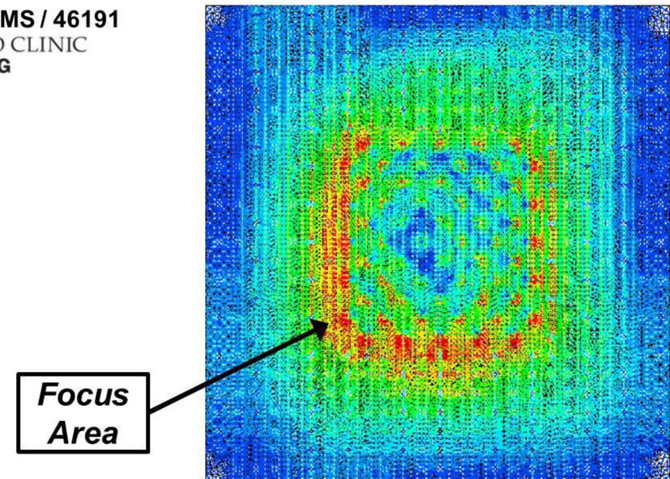
(b) Current Density – 80A Lumped Current Load



(c) Package Via Design

	uVia: La to Lb	uVia: C4 to C5
Name:	BV040La-b_SE_A	BV100C4-C5_SE_A
Drill Type:	Laser Micro	Laser Micro
Drill Diameter:	0.040	0.100
Inner Pad Diameter:	0.060	0.125
Top Pad Diameter:	NA	NA
Bottom Pad Diameter:	NA	NA
Antipad Style:	Circle	Circle
Antipad Diameter:	0.150	0.150

(d) Current Density – 80A Distributed Current Load



Example 2 – First Level Package: PDN DCIR (2)

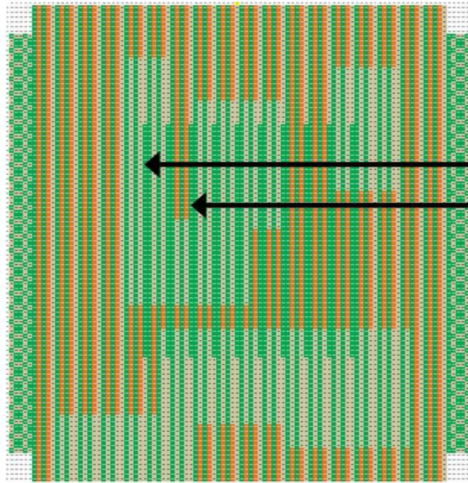
- Common practice is to use lumped current load – i.e. tie all micro-bumps together to singular current sink
  - Simple and straightforward compared to the tedious process of adding individual (per-bump) current sinks with PDN simulator GUI
  - Often applies inaccurate equipotential assumption to each micro-bump; hence voltage incorrectly bounded and current paths modified from reality
- IC designer may be able to provide accurate spatial current loading conditions to fine tune analysis assumptions
  - Processing script imports the pin current assignments to apply thousands of discrete sinks at each micro-bump

Example 2 – First Level Package: PDN DCIR (3)

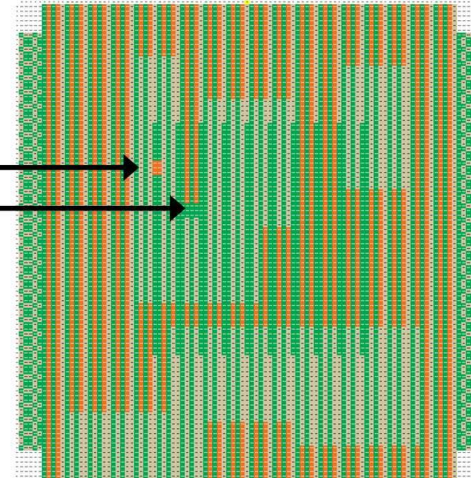
- Observed dramatic difference in current density gradient between lumped and distributed load conditions for sample package with same total current applied (80A)
  - Not an unexpected PDN result, but analysis was made much simpler and more accurate through scripting process
- Re-assigned nets on several micro-bumps in spreadsheet within “focus area” of extreme high current density
  - Recreated geometry using script with updated assignments
  - Quickly quantify improvement in focus area
  - Step and repeat as necessary given targeted areas of high-current consumption
  - Potentially use information to also influence IC design, if possible reconsider active device layout

POWER DELIVERY NETWORK DESIGN AUTOMATION - PACKAGE CURRENT DENSITY REDUCTION ANALYSIS RESULTS

(a) Package Microbump Pinout – Original Net Assignment



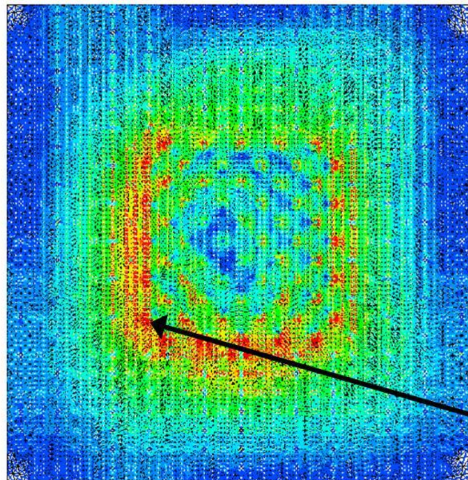
(b) Package Microbump Pinout – Modified Net Assignment



6 Pins Converted Ground to Power

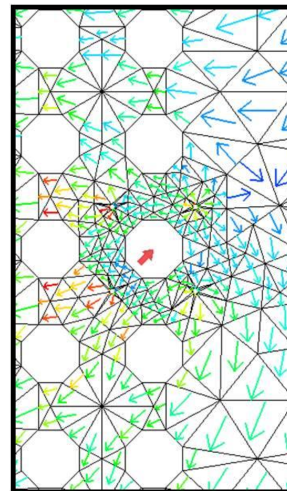
6 Pins Converted Power to Ground

(c) Current Density – 80A Distributed Current Load

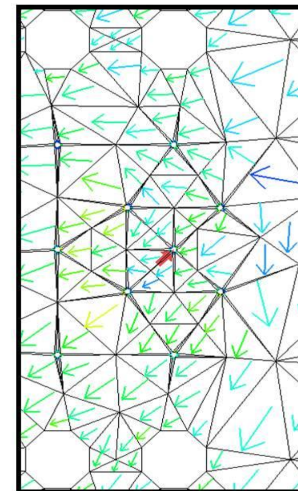


Focus Area

(d) Current Density in Focus Area



Original Net Assignment



Modified Net Assignment

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Concluding Remarks (1)

- As we presented in a 2016 SPI paper, passive PDN design trade-space is vast and multi-faceted
  - Considerations include: materials, packaging density, signal bandwidth, decoupling capacitors, pinfield breakouts, via technology, fabricator capability, stackup construction, net assignments, stringent impedance requirements, etc.
  - Simultaneously satisfying SI and PI requirements in a singular design is a challenge
- Efficient, pre-layout PDN design process demonstrated
  - Exploits scripting capability in 3D EM solvers
  - "What if" PDN design scenarios evaluated quickly without need for CAD resources

Concluding Remarks (2)

- Examples shown were intended to demonstrate need for, and utility of, scripting process – intentionally simplistic
- Application of pre-layout analysis process can be extrapolated to much more complex design conditions
  - Multiple high-power ASICs attached to single carrier PCB with several multi-phase regulators providing core voltages
    - Emulates directional current flow to more accurately capture lateral package current density in DCIR simulation
  - Thousands of discrete capacitors with potential blockage from higher priority devices (connectors, memory, etc.)
  - Electro-thermal co-simulation in coupled analysis to evaluate thermal power dissipation and temperature gradients in passive packaging caused by Joule heating

THANK YOU!

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