An IBIS-like Modelling For Power/Ground Noise Induced Jitter Under Simultaneous Switching Outputs (SSO)

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PRESENTATION OUTLINE

1. Introduction
2. Noise and Jitter
3. Analysis of P/G Bouncing under SSO
4. Previous/Related Work
5. IBIS-like Model Derivation and Extraction
6. Model Validation and Jitter Assessment
7. Conclusion

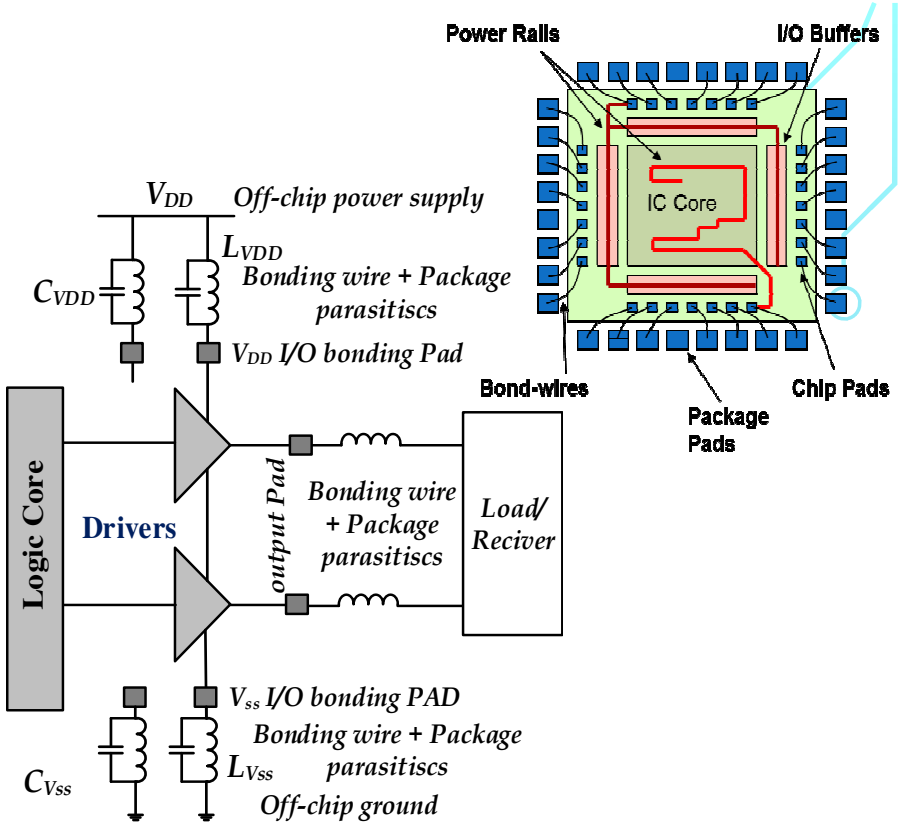
NOISE AND JITTER

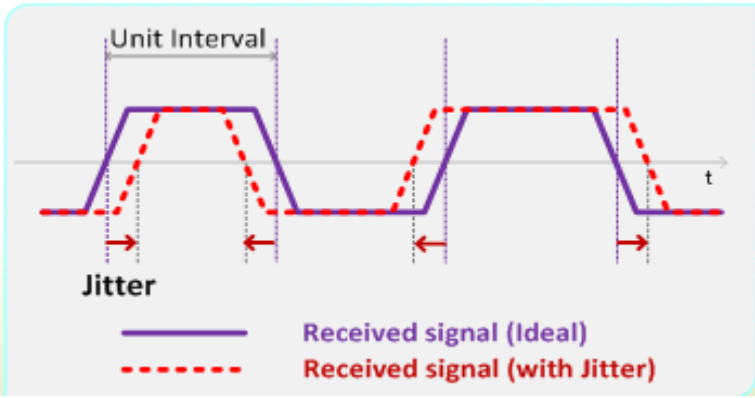
Three main causes of power and ground supply noise:

- Power distribution network.
- High speed current Ldi/dt.
- Simultaneous switching output buffer.

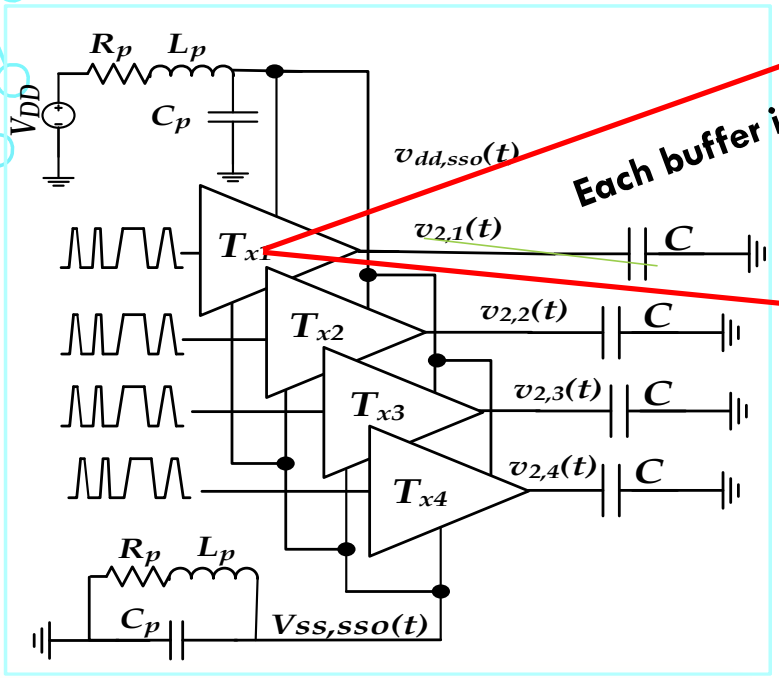
Jitter is one of the important timing metrics in high-speed systems.

- Is the timing variations in the transition edges from their ideal positions.
- Total jitter (TJ) in a circuit or system can be categorized into two major categories as random jitter (RJ) and deterministic jitter (DJ).

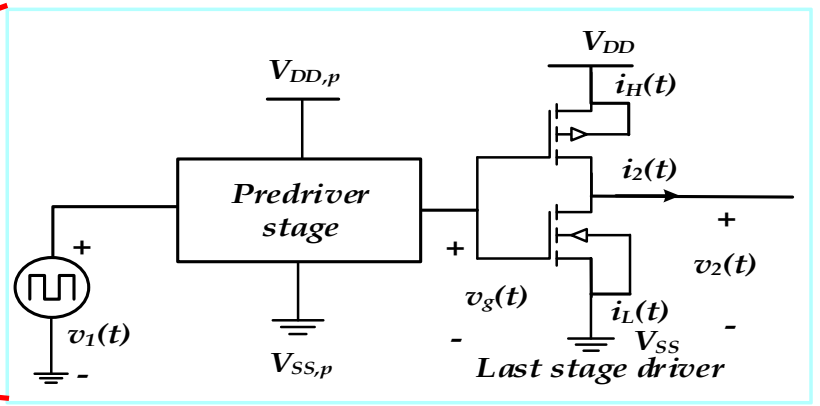




ANALYSIS OF P/G BOUNCING UNDER SSO: SIMULATION



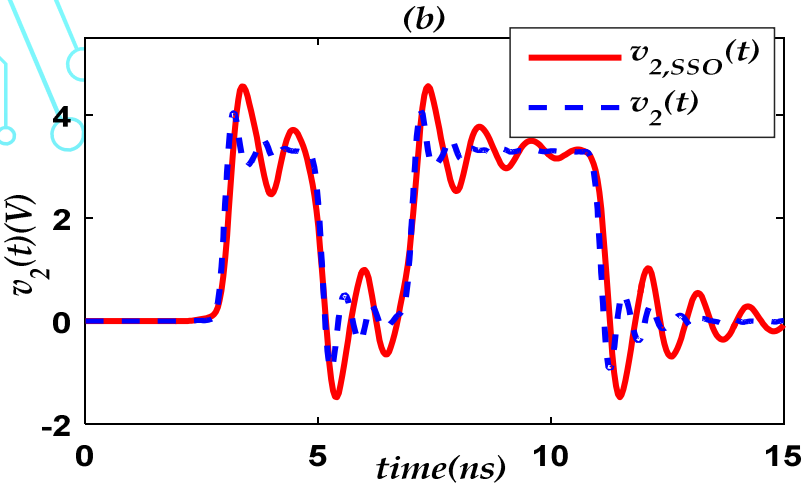
Each buffer is structured as

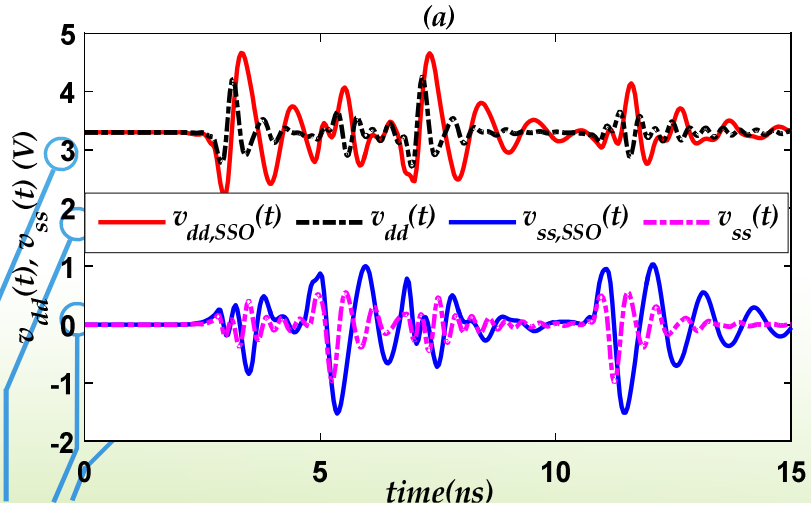


Circuit package parameters:
$R_p = 20\ m\Omega, L_p = 2\ nH, C_p = 2\ pF,$
$C = 2\ pF.$

- The driver is having **four cascaded inverters** in **series** and designed in $0.35\mu m$ technology of TSMC.
- The **first three inverters:** The pre-driver stage. Powered by constant power $V_{DD,p} = 3.3\ V, V_{SS,p} = 0\ V.$
- These supplies are **isolated** from the ones used for powering the driver's last stage.

ANALYSIS OF P/G BOUNCING UNDER SSO: RESULTS





- SSO increases the di/dt noise ➔ Larger variations in $v_{ss,sso}(t)$ and $v_{dd,sso}(t)$.

➔ the output voltage, $v_2(t)$ overshoot -1.46 V and undershot 4.56 V.

➔ High output logic level $\Delta v_{dd,sso}/V_{DD}$ is 63.45%

➔ Low logic level is $\Delta v_{ss,sso}/V_{DD}$ 73.84%.

SSO noise Induces both **amplitude** and **jitter (timing)** distortions on the **output signal.**

Previous/Related Work

Previous works :

- Assume the perturbation analysis of the P/G voltage, where linear approximation of the I-V (C-V) functions can be used because the biasing region of the pull-up and pull down transistors of the driver's last stage will not be severely affected.

➔Therefore, **a small signal transistor model** for P/G induced jitter can be used by including the linear capacitive effects.

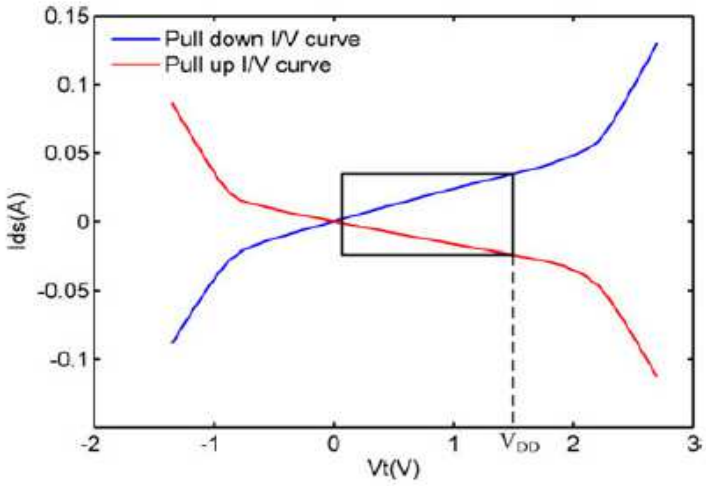


Fig. 5. Pull-down and pull-up *I/V* curve from IBIS model.

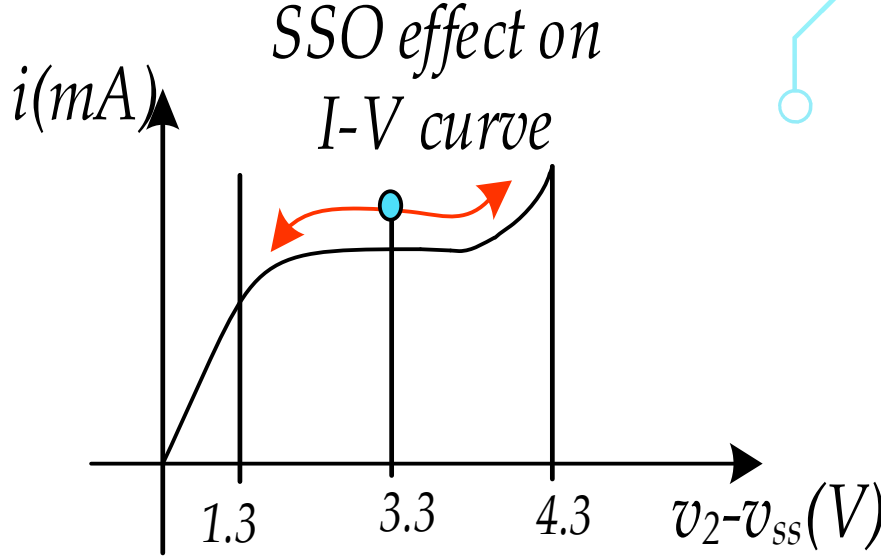
J. N. Tripathi, P. Arora, H. Shrimali and R. Achar, "Efficient Jitter Analysis for a Chain of CMOS Inverters", IEEE Tran. EMC, pp. 1 – 11, Nov. 2018.

X. Chu, C. Hwang, J. Fan and Y. Li, "Analytic Calculation of Jitter Induced by Power and Ground Noise Based on IBIS I/V Curve", IEEE Tran. EMC, pp. 468 – 477, vol. 60, no. 2, 2018.

Problem Statement

The SSO scenario affects the **biasing** and **working regimes** of the **PU** and **PD** transistors forming the last stage of the driver (e.g. linear or saturation).

➔A fully **nonlinear model** for the **driver's last stage** is **required** for accurately **capturing** the P/G induced **jitter** and **distortions.**



➔**<u>Considering ONLY</u>** the **IBIS I-V curves** that **capture** the **instantaneous static distortions of the P/G variation** affects the **prediction accuracy** of **jitter** because of **the overlooked pull-up and pull-down capacitances, (C_H and C_L, respectively).**

X. Chu, C. Hwang, J. Fan and Y. Li, "Analytic Calculation of Jitter Induced by Power and Ground Noise Based on IBIS I/V Curve", IEEE Tran. EMC, pp. 468 – 477, vol. 60, no. 2, 2018.

Model Derivation and Extraction

IBIS Model Derivation

- The nonlinear dynamic electrical behaviors of I/O buffer circuit while considering the P/G voltage variables :

$$i_2(t) = w_L(t) F_L\left(\mathrm{x_{dd}(t)}, \frac{d\mathrm{x}_{dd}(t)}{dt}\right) + w_H(t) F_H\left(\mathrm{x_{ss}(t)}, \frac{d\mathrm{x}_{ss}(t)}{dt}\right) \quad (1)$$

Switching Time Signals

$$\mathrm{x}_{dd}(t) = v_{dd}(t) - v_2(t) \qquad \mathrm{x}_{ss}(t) = v_2(t) - v_{ss}(t)$$

Regressor vector applied to the $F_L(\cdot)$ and $F_H(\cdot)$ functions

$F_L(\cdot)$ and $F_H(\cdot)$ model the nonlinear dynamic output admittances of the driver's last stage under low and high input logic levels.

This model takes into account:

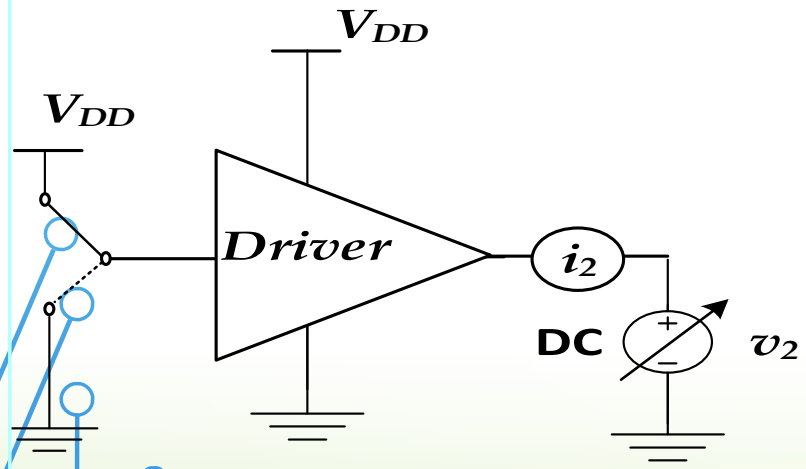
- The I-V static contribution of the P/G voltage fluctuation of the last stage.
- The delay introduced by the PU and PD capacitances ➔ represented by the voltage dependent capacitance (C-V).

Model Extraction : I-V Functions

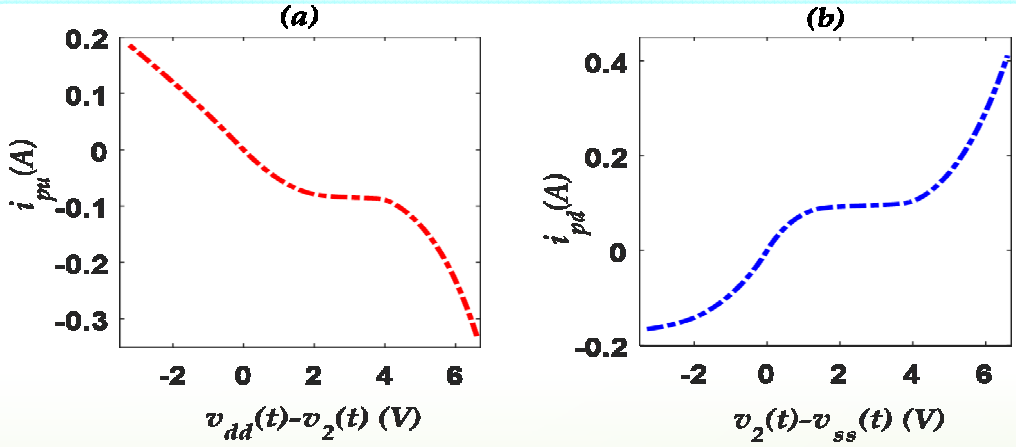
- **The nonlinear I-V relationships:**

$$\begin{cases} i_H(t) = I_H\left(\mathrm{x_{dd}(t)}\right) + C_H \dfrac{dx_{dd}(t)}{dt} \\ i_L(t) = I_L\left(\mathrm{x_{ss}(t)}\right) + C_L \dfrac{dx_{ss}(t)}{dt} \end{cases} \qquad (2)$$

$I_H(.)$ and $I_L(.)$ functions model the nonlinear I-V relationship of the last stage formed by the PU and PD MOSFET transistors and the protection diodes.

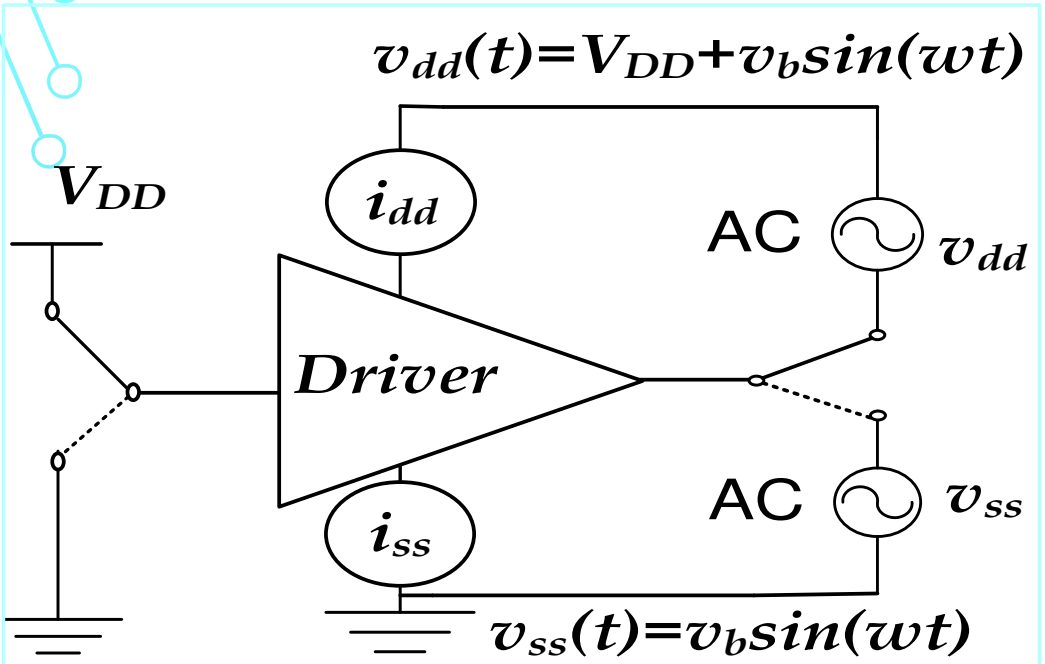


The sweep range of v_2 is $[-V_{DD}, 2V_{DD}]$ as recommended by the IBIS specification



Static dc I-V characteristic according to IBIS specifications (a) PU I-V curve, (b) PD I-V curve.

Model Extraction : C-V Function



$C_H(v_b)=imag(Y_{11,H})/w$

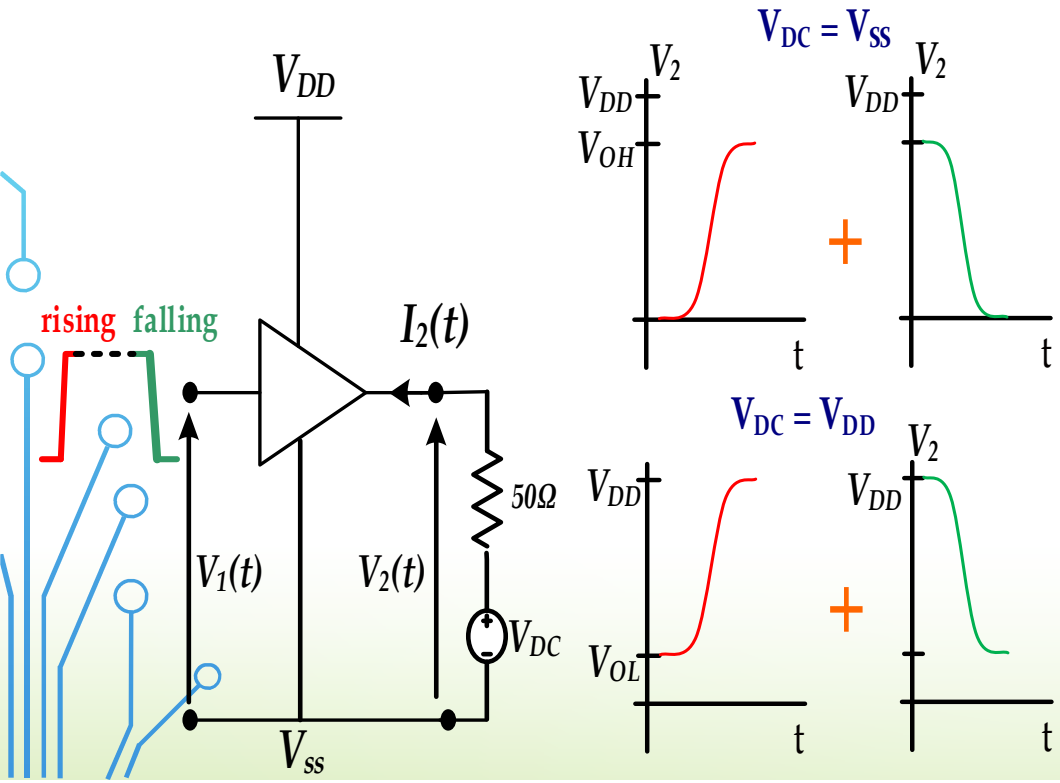
$C_L(v_b)=imag(Y_{11,L})/w$

v_b sweep range is $[-V_{DD}, 2V_{DD}]$

- The C_H and C_L, capture the dynamic distortion of the P/G variation on the output signals.
- The capacitive effects improves the accuracy of the jitter prediction induced by the P/G voltage variations.

Model Extraction : switching timing signals $w_L(t)$ and $w_H(t)$

Setup for switching timing signals extraction



The $w_L(t)$ and $w_H(t)$ functions :

- ✓ capture the predriver's input-output timing distortions extracted by means of the two equations with two unknowns (2E2U) algorithm

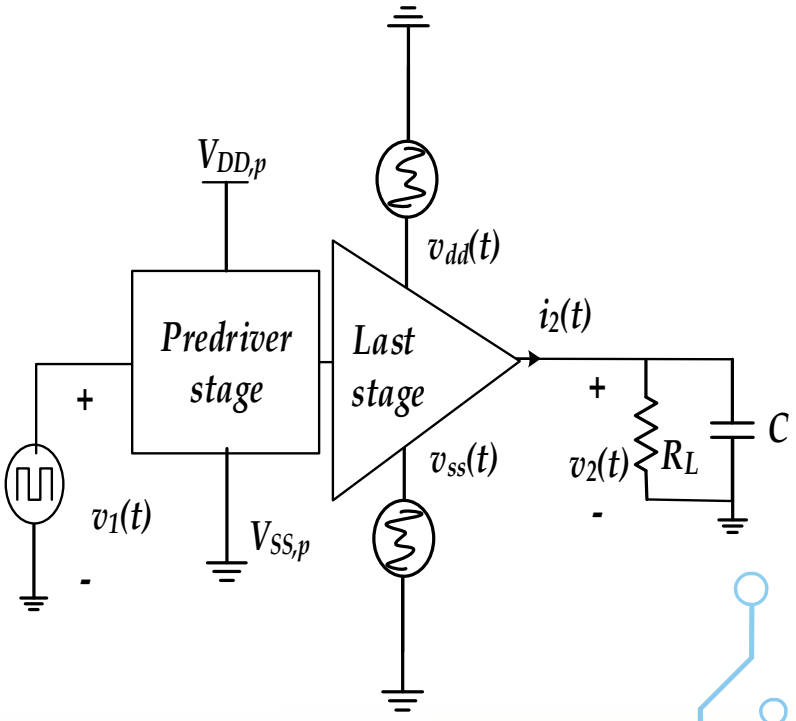
$$\begin{bmatrix} w_L^n(t) \\ w_H^n(t) \end{bmatrix} = \begin{bmatrix} I_{L,b}^n(t) & I_{H,b}^n(t) \\ I_{L,a}^n(t) & I_{H,a}^n(t) \end{bmatrix}^{-1} \cdot \begin{bmatrix} I_{2,a}^n(t) \\ I_{2,b}^n(t) \end{bmatrix}$$

- ✓ The $w_L(t)$ and $w_H(t)$ functions are assumed to be mildly affected by the P/G bouncing effect

Model Validation and Jitter Assessment

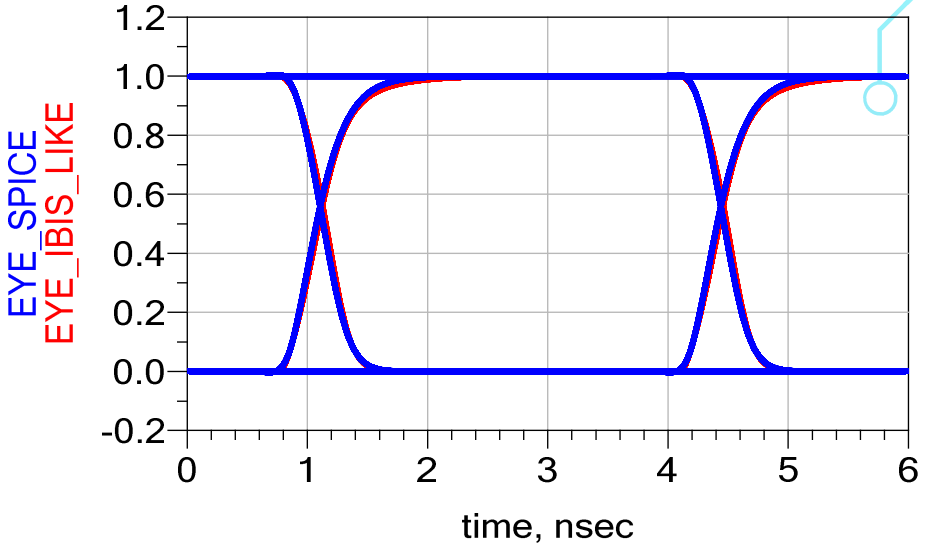
Model Validation and Implementation

- The I-V and C-V functions were implemented as look-up tables in MATLAB Simulink time domain solver.
- The pull up and pull down capacitances are connected between the power-output-pin and the ground-output-pin.
- The $w_L(t)$ and $w_H(t)$ functions are computed offline and implemented as piece-wise linear signal using the repeating sequence block.
- Three test cases was performed for predicting jitter under constant and P/G voltage variations.



Test case 1: Eye Diagram prediction under constant P/G voltage

- The developed model is able to accurately predict the **inherent drive's jitter distortions** under constant P/G supply voltages.
  - ✓ **The prediction error of eye's jitter and width are 0.34% and 0.15%.**
- These measurements were carried out under :
  - ✓ 40-60% eye boundary, which indicates the measurement region between eye crossing points
  - ✓ the eye threshold levels are the 20% to 80% points on the rising and falling transitions.



Jitter performance: IBIS-like vs. Spice-level models

Model / Performance	Spice-based	IBIS-like
Eye jitter (pp) (ps)	59.56	59.30
Eye width (ns)	3.33	3.335
Eye height (V)	3.29	3.284

Test case 2: Timing signal prediction under two-tone P/G signals

- $v_{dd}(t)$ and $v_{ss}(t)$ are represented by:

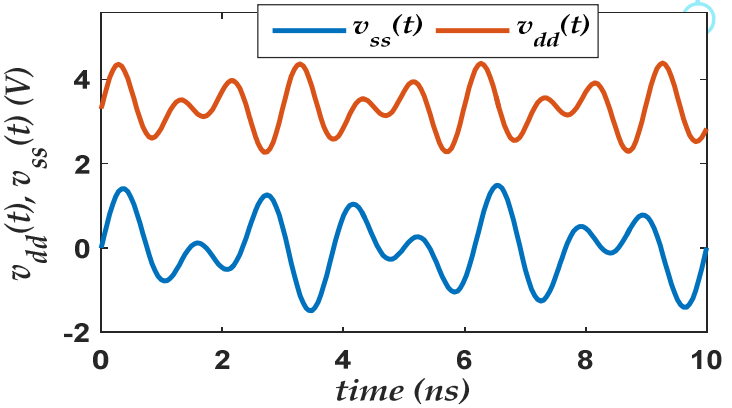
$$\begin{cases} v_{dd}(t) = V_{DD} + a_1\, sin(2\pi f_1 t) + a_2\, sin(2\pi f_2 t) \\ v_{ss}(t) = a_3 sin(2\pi f_3 t) + a_4 sin(2\pi f_4 t) \end{cases}$$

where $f_1 = 1\ GHz$, $a_1 = 0.6\ V$, $a_2 = 0.5\ V$, $f_2 = 670\ MHz$, $f_3 = 550\ MHz$, $a_3 = 0.5\ V$, $a_4 = 0.8\ V$ and $f_4 = 800\ MHz$.

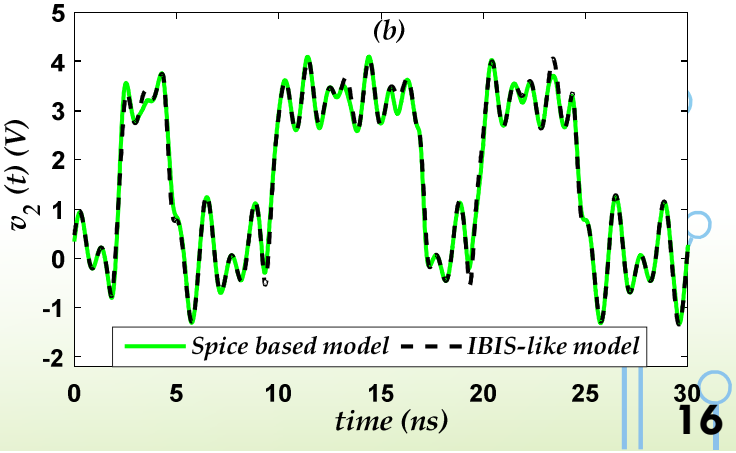
- This P/G validation signals ensure almost 66.66% peak-to-peak (pp) of the P/G voltage variations around the nominal voltage supply V_{DD}.

➔The error was less than 0.47 V which represents less than 8% of the of $v_{2,pp}(t)$ (e.g. peak-to-peak).

P/G voltage waveforms used in test case # 2



Prediction of the $v_2(t)$ waveform.



Test case 3: Eye diagram prediction under sinusoidal P/G variations

The model is validates by superimposing 4 sinusoidal signals at the P/G terminals.

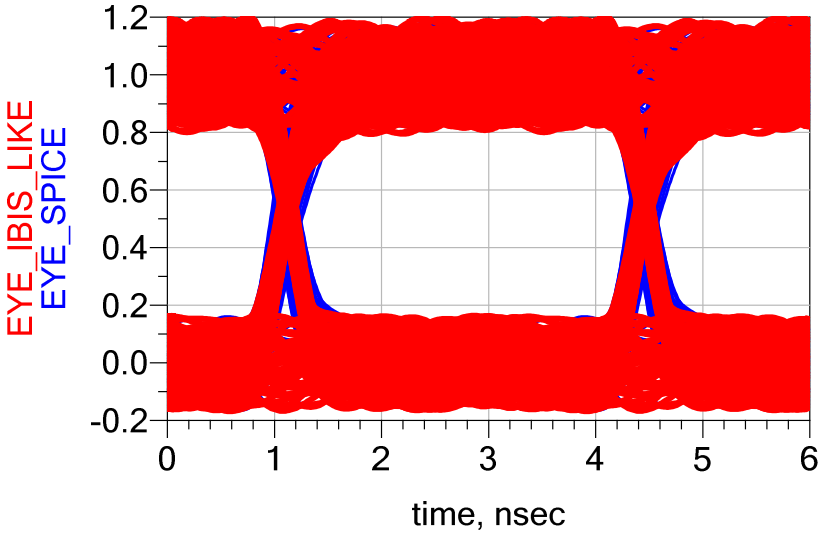
$$\begin{cases} v_{dd}(t) = V_{DD} + \sum_{i=1}^{4} a_i \sin(2\pi f_{di} t) \\ v_{ss}(t) = \sum_{i=1}^{4} b_i \sin(2\pi f_{si} t) \end{cases}$$

- **The amplitude and frequency parameters:**

$a_i = \{0.4\,, 0.05, 0.2, 0.1\}\,V;\ f_{di}\{328, 100, 625, 833\}\,MHz,$
$b_i = \{0.2\,, 0.3, 0.1, 0.1\}\,V; f_{si} = \{250, 370, 870, 628\}\,MHz.$

The prediction accuracy of IBIS-like model :

- **eye's jitter is 7.06 %**
- **Eye width is 2.59%**



Jitter performance: IBIS-like vs. Spice-level models

Model / Performance	Spice-based	IBIS-like
Eye jitter (pp) (ps)	257.30	240.33
Eye width (ns)	3.08	3.16
Eye height (V)	2.21	2.13

CONCLUSION

- This work has evaluated the performance of the proposed IBIS-like model formulation and extraction for predicting the P/G voltage variations in different validation scenarios that emulate the SSO case where the fast bouncing P/G voltage supplies are large in magnitude.
  - A nonlinear I-V and C-V model for the PU and PD devices are required to capture the static effects of the variation of the supply voltages.
  - The simple linear capacitive model should be extended to a nonlinear case while the model should be validated with higher clock rates to assess its jitter predicting capabilities.
  - A generic I/O buffer circuit structure should be considered where the pre-driver's and last stage are powered by the same voltage supplies.