Analysis of Jitter for a Chain-of-Inverters including On-chip Interconnects

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Outline

- Introduction
- Power Supply Induced Jitter (PSIJ)
- Semi-analytical Modeling: EMPSIJ
- Chain-of-Inverters with interconnects
- Results
- Conclusion

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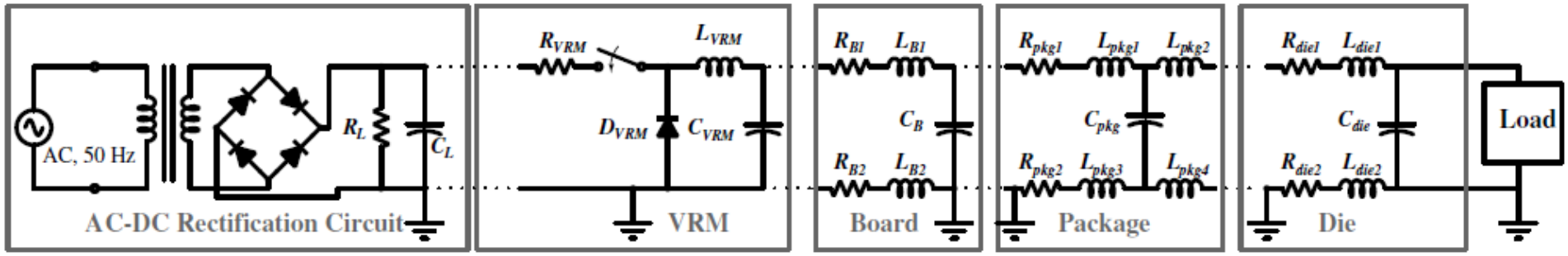
Introduction

- Low power, smaller area, higher switching frequencies.
  - Leads to voltage fluctuations in PDNs.
  - IR-drop, Ldi/dt noise, LC resonance, Crosstalk, Electromagnetic interference.



A typical Power Distribution Network (PDN)

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Jitter

- Low power, smaller area, higher switching frequencies.
- Can be categorized in Random Jitter (RJ) and Deterministic Jitter (DJ).
- DJ → Inter-symbol Interference (ISI), Simultaneous Switching Noise (SSN), Ground Bounce, EMI, etc.
- Jitter budgets are defined to maintain timing margins.

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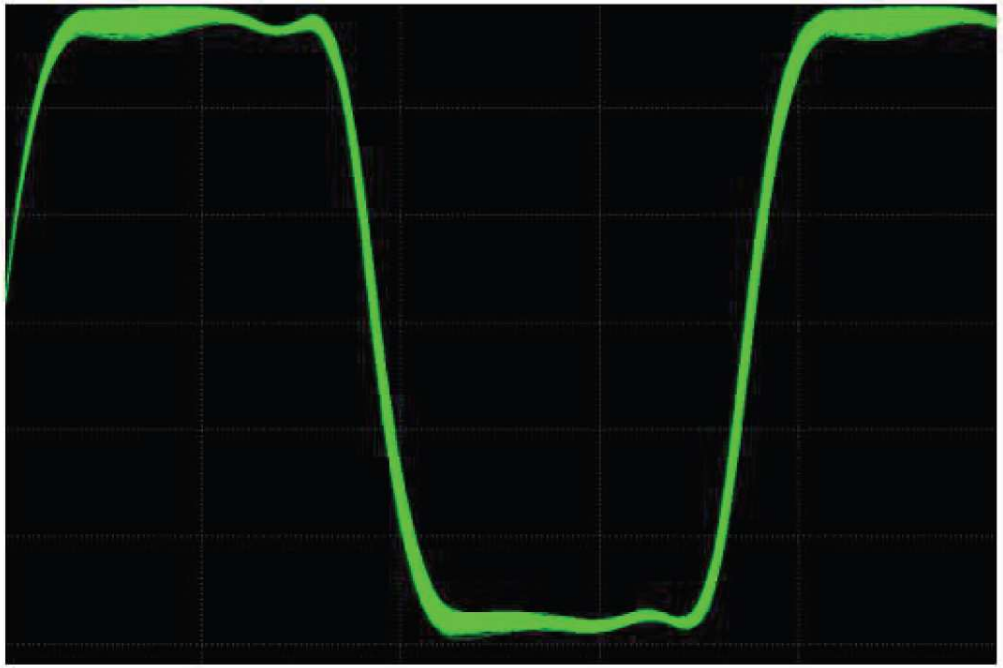
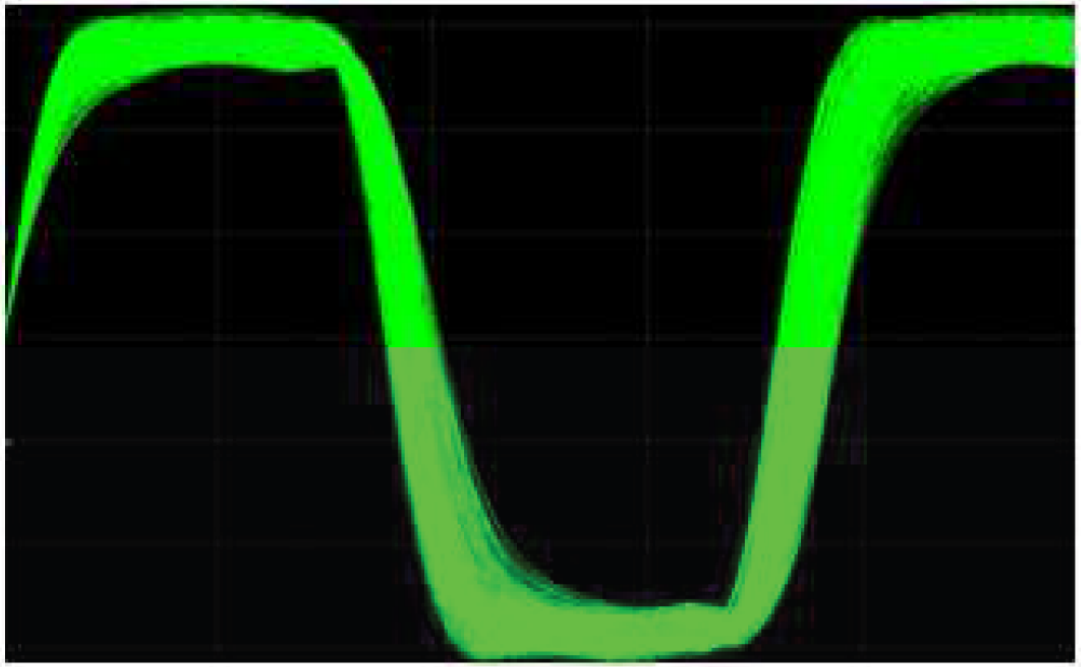
Power Supply Induced Jitter

Worst Case PVT SS-40



Period Jitter: -16.1ps/6.3ps

Worst Case PVT SS-40



Period Jitter: -91.6ps/110.9ps

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Recent Work

- Slope based Approaches
  - J. Kim et al., IEEE EMC Symp., Aug. 2011.
  - J. N. Tripathi et al., EMPSIJ, T-CPMT, Oct. 2017.
- Delay-based Approaches
  - X. J. Wang and T. Kwasniewski, TEMC, Apr. 2016.
  - J. N. Tripathi et al., TVLSI, Oct. 2017.
- Statistical methods:
  - J. Kim et al., IEEE TCAS-1, Jul. 2014.
- Via IBIS Models
  - X. Chu et al., TEMC, Nov. 2017.
- Numerical Method
  - J. N. Tripathi and F. Canavero, IEEE MWCL, Dec. 2017.

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EMPSIJ

- Efficient Modeling of Power Supply Induced Jitter (EMPSIJ). → TCPMT, Oct. 2017.
- Slope based Semi-analytical approach.
- Requires only one-bit simulation to evaluate the slope (β).
- TIE for k^{th} bit can be calculated as:

$$\mathrm{TIE}^k = J_r^k = \frac{(v_{r_n}^k)_{t_m}}{\beta}$$

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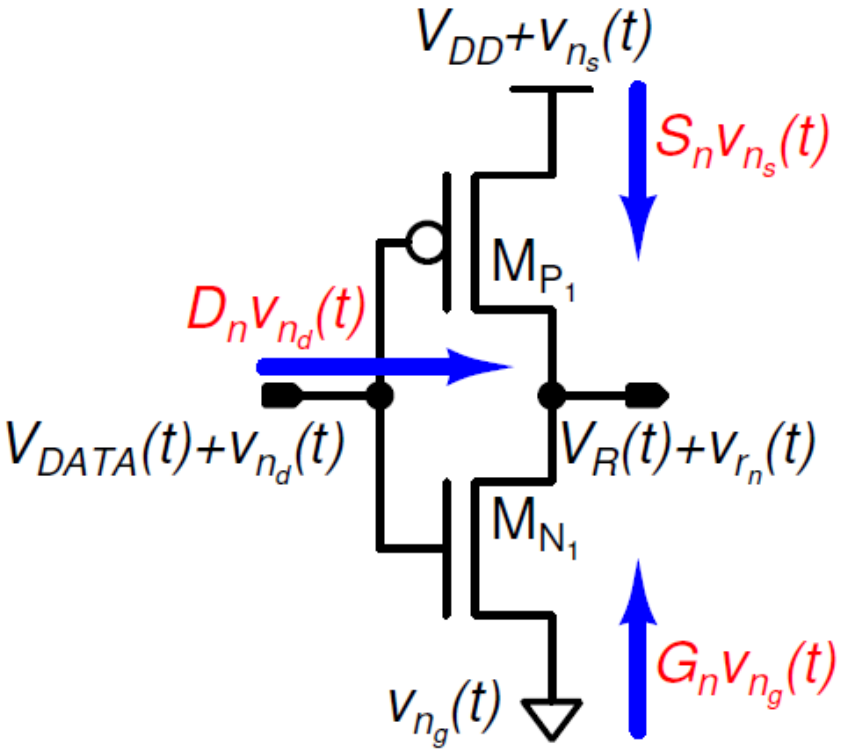
Power Supply Noise in a CMOS Inverter

- S_n, G_n, and D_n are the transfer functions of respective paths.
- $v_{ns}(\mathrm{t})$, $v_{ng}(\mathrm{t})$ and $v_{nd}(\mathrm{t})$ are input noise components.
- $v_{DATA}(\mathrm{t})$ and $v_R(\mathrm{t})$ are the input and output data signals.
- $v_{rn}(\mathrm{t})$ is the total output noise.



PSN Components and their paths in CMOS inverter.

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PSN Components

- The total output noise,

$$v_{r_n}(t) = v_{r_s}(t) + v_{r_g}(t) + v_{r_d}(t)$$

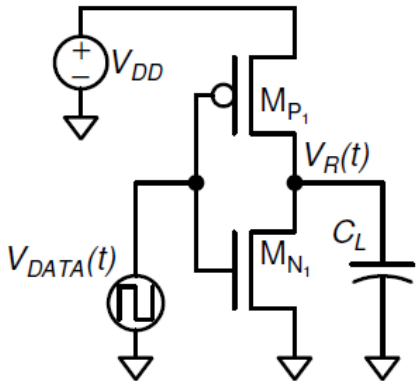
- Where,

$$v_{r_s}(t) = S_n v_{n_s}(t)$$

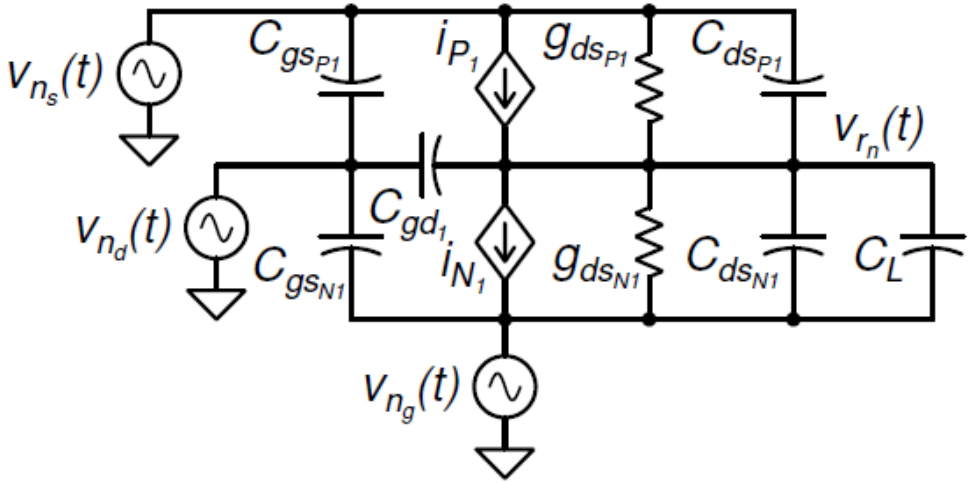
$$v_{r_g}(t) = G_n v_{n_g}(t)$$

$$v_{r_d}(t) = D_n v_{n_d}(t)$$

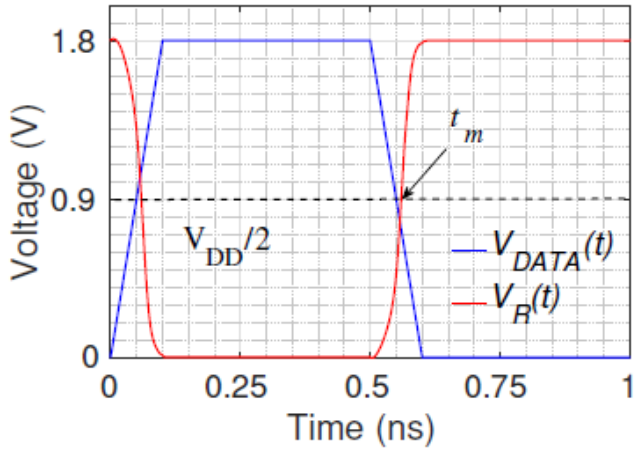
Large Signal Analysis and Small-signal Model



Large signal model



Small-signal model



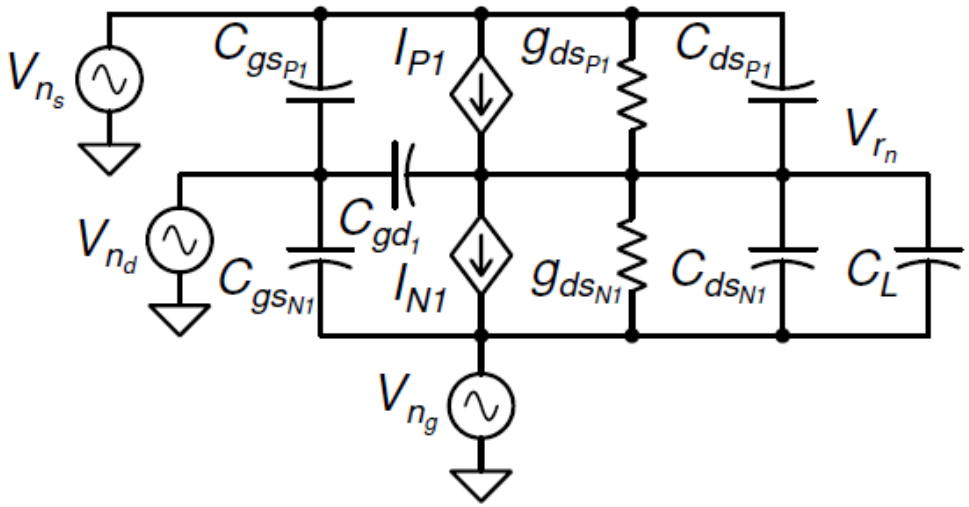
Input and output waveforms

Noise Transfer Functions

$$S_n = \frac{V_{r_s}}{V_{n_s}} = \frac{g_{ds_P} + g_{m_P}}{g_{ds_P} + g_{ds_N} + j\omega_s(C_{gd} + C_{ds_P} + C_{ds_N} + C_L)}$$

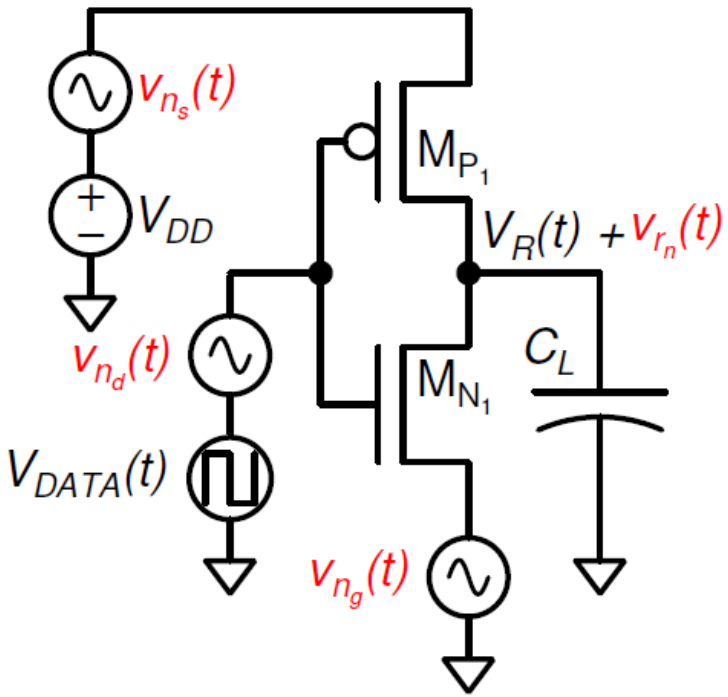
$$G_n = \frac{V_{r_g}}{V_{n_g}} = \frac{g_{ds_N} + g_{m_N}}{g_{ds_P} + g_{ds_N} + j\omega_g(C_{gd} + C_{ds_P} + C_{ds_N} + C_L)}$$

$$D_n = \frac{V_{r_d}}{V_{n_d}} = \frac{j\omega_d C_{gd} - g_{m_P} - g_{m_N}}{g_{ds_P} + g_{ds_N} + j\omega_d(C_{gd} + C_{ds_P} + C_{ds_N} + C_L)}$$



Small-signal model in frequency domain.

Noise Transfer Functions



Inverter with noise sources.

Input noise

$$v_{n_s}(t) = A_s \sin(2\pi f_s t + \phi_s)$$

$$v_{n_d}(t) = A_d \sin(2\pi f_d t + \phi_d)$$

$$v_{n_g}(t) = A_g \sin(2\pi f_g t + \phi_g)$$

Output noise

$$v_{r_s}(t) = |S_n| A_s \sin(2\pi f_s t + \phi_s + \angle S_n)$$

$$v_{r_g}(t) = |G_n| A_g \sin(2\pi f_g t + \phi_g + \angle G_n)$$

$$v_{r_d}(t) = |D_n| A_d \sin(2\pi f_d t + \phi_d + \angle D_n)$$

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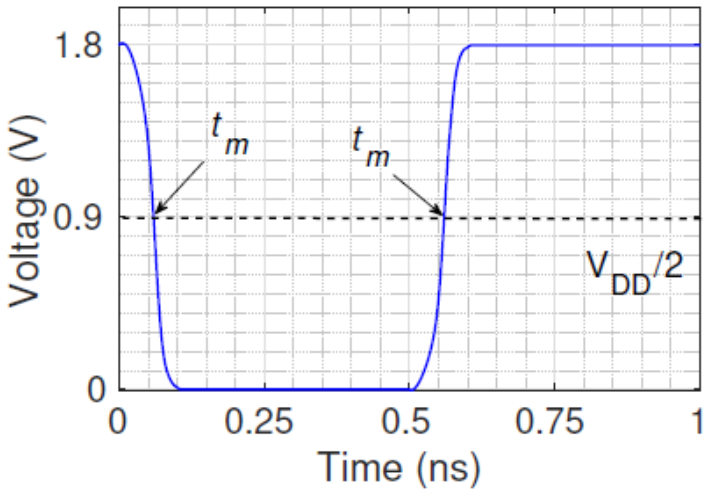
Estimation of TIE and PSIJ

$$v_{r_n}(t_m) = v_{r_s}(t_m) + v_{r_g}(t_m) + v_{r_d}(t_m)$$



$$J_r = \frac{v_{r_n}(t_m)}{\alpha_{t_m}}$$

$v_{r_n}(t_m)$ - Noise amplitude at t_m

α_{t_m} - Slope at t_m

$$J_{PP} = \frac{max[v_{r_n}(t_m)] - min[v_{r_n}(t_m)]}{\alpha_{t_m}}$$

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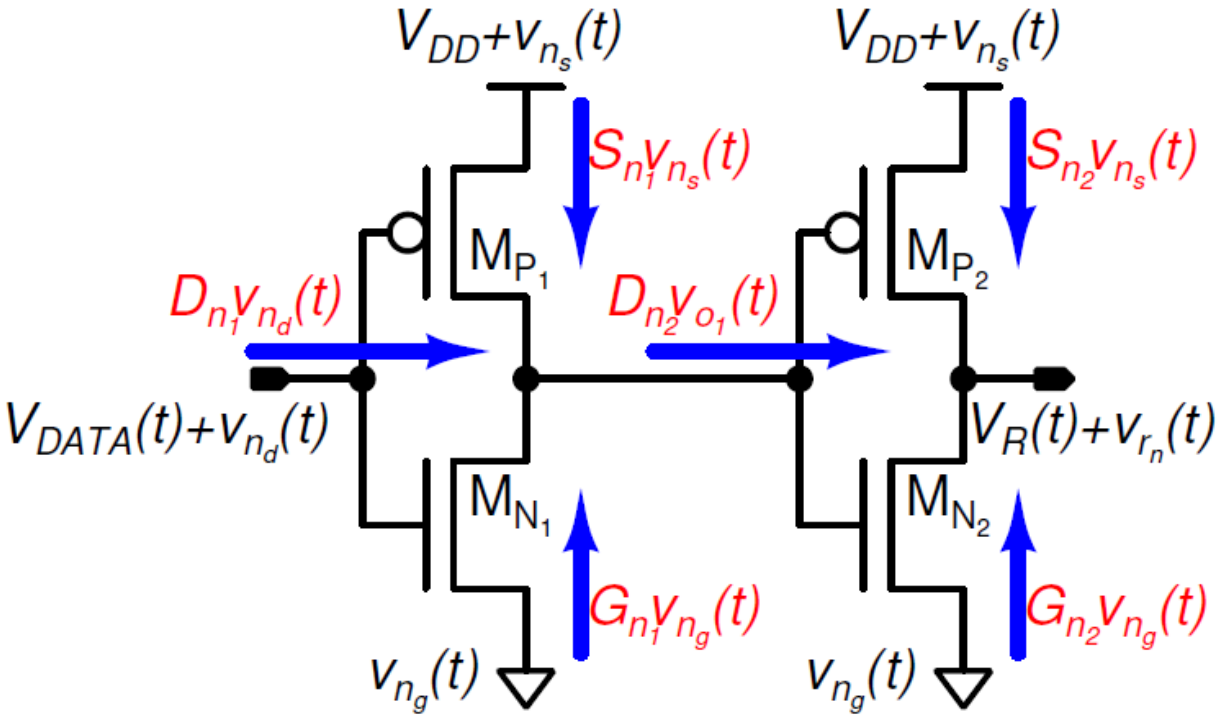
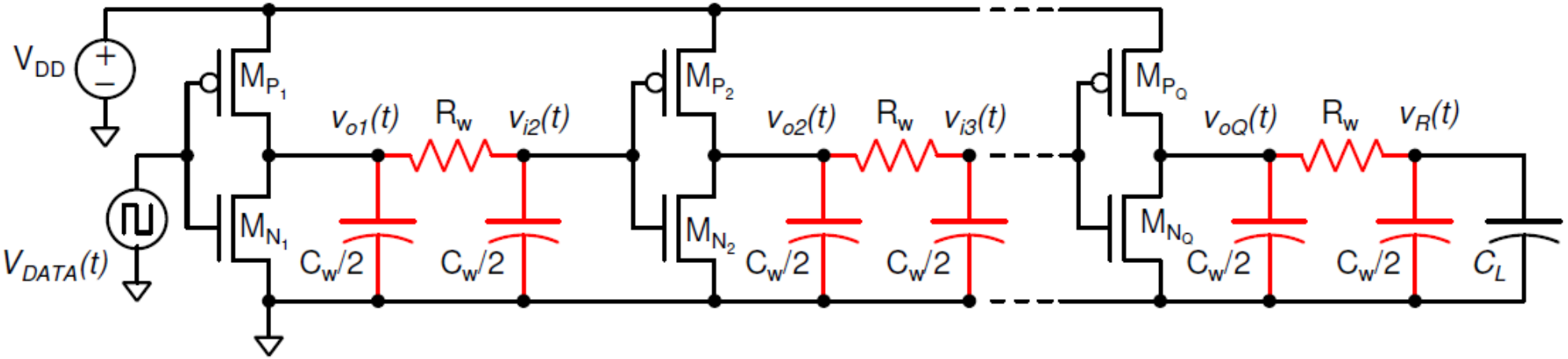
PSN in Chain of Inverters



PSN Components and their paths in two cascaded inverters.

Chain of Inverters with Interconnect



Chain of Inverters with On-Chip Interconnects

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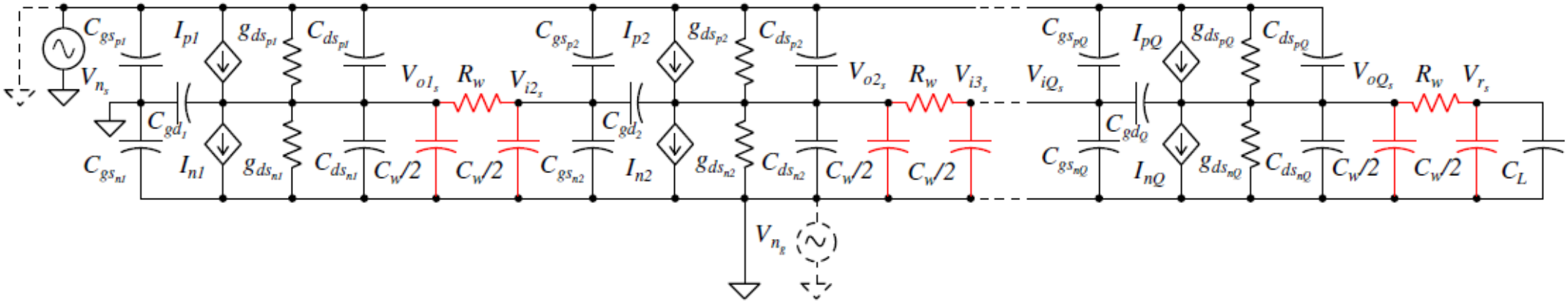
Noise Transfer Functions



$$d_{1_s} V_{o1_s} + u_{1_s} V_{i2_s} = b_{1_s} V_{n_s}$$

$$l_{2_s} V_{o1_s} + d_{2_s} V_{i2_s} + u_{2_s} V_{o2_s} = b_{2_s} V_{n_s}$$

$$\vdots$$

$$l_{(2Q)_s} V_{(oQ)_s} + d_{(2Q)_s} V_{r_n} = b_{(2Q)_s} V_{n_s}$$

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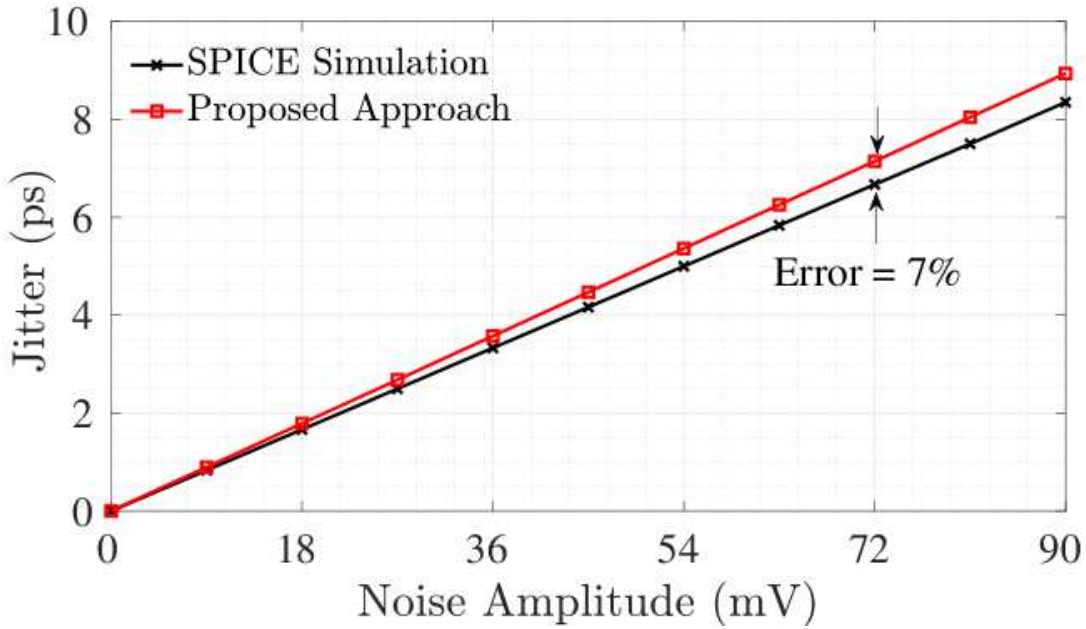
Noise Transfer Functions

- $\mathbf{X}_s(j\omega_s) = \mathbf{A}_s(j\omega_s)^{-1}\mathbf{B}_s(j\omega_s)V_{n_s}(j\omega_s)$
- $\mathbf{X}_g(j\omega_g) = \mathbf{A}_g(j\omega_s)^{-1}\mathbf{B}_g(j\omega_s)V_{n_g}(j\omega_g)$

where,

$$\mathbf{X}_s(j\omega_s) = \begin{bmatrix} V_{o1_s}(j\omega_s) \\ V_{o2_s}(j\omega_s) \\ \vdots \\ V_{o(2Q-1)_s}(j\omega_s) \\ V_{r_s}(j\omega_s) \end{bmatrix}; \ \mathbf{B}_s(j\omega_s) = \begin{bmatrix} b_{1_s}(j\omega_s) \\ b_{2_s}(j\omega_s) \\ \vdots \\ b_{(2Q-1)_s}(j\omega_s) \\ b_{2Q_s}(j\omega_s) \end{bmatrix}$$

Results



Ex-1: Chain of inverters with 5 stages

Technology used	BiCMOS 55nm (STMicroelectronics)
Supply voltage	1.8 V
Input data rate	2 Gbps

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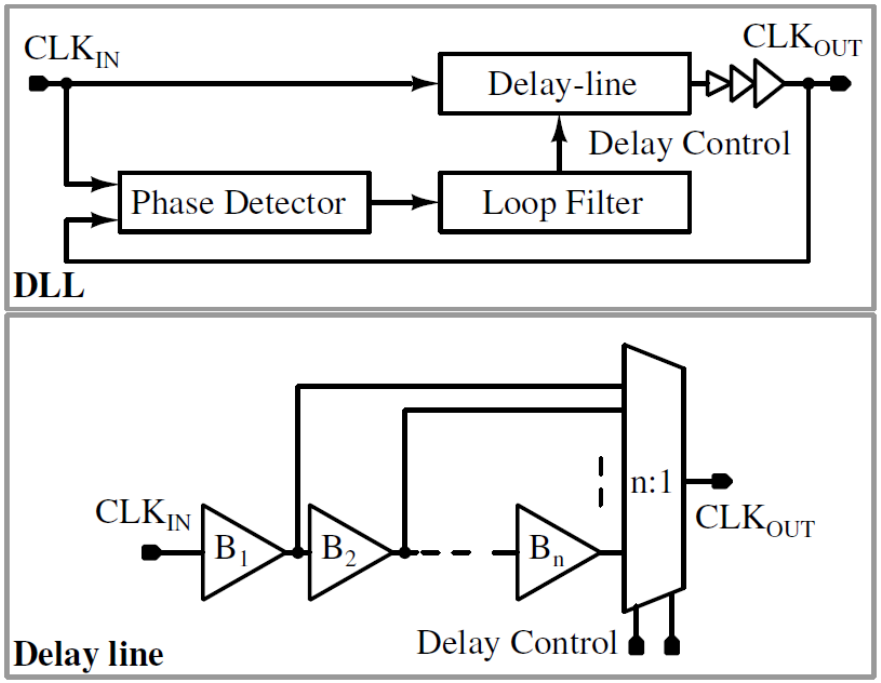
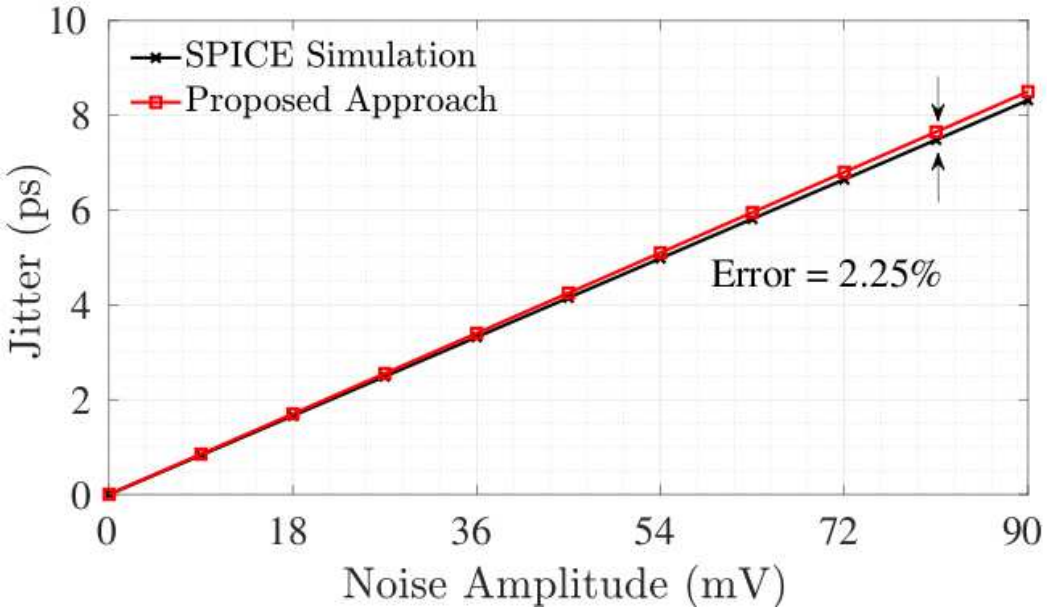
Results



Ex-2: Delay Locked Loop



Ex-2: Tapered buffer with 5 stages

Technology used	BiCMOS 55nm (STMicroelectronics)
Supply voltage	1.8 V
Input data rate	2 Gbps

Results

Example	Approach	CPU Time	Speed-up
Example-1	Conventional	8 min. 34 sec.	~123
	Proposed	4.17 sec.	
Example-2	Conventional	12 min. 5 sec.	~133
	Proposed	5.44 sec.	

Summary/Conclusion

- Faster estimation for PSIJ is required to reduced design cycle of SoCs.
- Semi-analytical methods can be useful for the same.
- Effects of off-chip and on-chip interconnects on jitter should be studied thoroughly to avoid the complications in meeting the specifications of overall timing uncertainty!

Thank You.