INFLUENCE OF DIFFERENT DIGITAL POWER SUPPLY LAYOUT STYLES ON THE EME OF ICS WITH RESPECT TO PROCESS VARIATIONS

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OVERVIEW

- Standard digital layout
- Test chip
- Process variations
- Measurement
- Conclusion
STANDARD DIGITAL LAYOUT

Standard cell/standard cell rows
STANDARD DIGITAL LAYOUT

standard cell/standard cell rows

VDD/VSS power stripes

digital core/filler cells

VDD/VSS power rings
STANDARD DIGITAL LAYOUT

- VDD/VSS power stripes
- Digital core/filler cells
- VDD/VSS power rings
STANDARD DIGITAL LAYOUT

- VDD/VSS power rings
- Digital core/filler cells
- VDD/VSS power stripes
Delta sigma digital-to-analog converter (ΔΣ-DAC)
Delta sigma digital-to-analog converter (ΔΣ-DAC)

ΔΣ-modulator is realized as a 3rd order CIFB structure

CIFB → cascade-of-integrators feedback
TEST CHIP

Top layout

250nm CMOS technology
approx. 32mm²
### TEST CHIP

**Top layout**

![Top layout image]

<table>
<thead>
<tr>
<th>Core</th>
<th>Power Ring Width (VDD or VSS)</th>
<th>Arrangement</th>
<th>Filler Cells Capacitance</th>
<th>Power Stripes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIG1</td>
<td>84µm</td>
<td>stacked</td>
<td>with</td>
<td>yes</td>
</tr>
<tr>
<td>DIG2</td>
<td>84µm</td>
<td>stacked</td>
<td>without</td>
<td>yes</td>
</tr>
<tr>
<td>DIG3</td>
<td>84µm</td>
<td>flattened</td>
<td>with</td>
<td>yes</td>
</tr>
<tr>
<td>DIG4</td>
<td>84µm</td>
<td>flattened</td>
<td>without</td>
<td>yes</td>
</tr>
<tr>
<td>DIG5</td>
<td>8.4µm</td>
<td>stacked</td>
<td>with</td>
<td>yes</td>
</tr>
<tr>
<td>DIG6</td>
<td>8.4µm</td>
<td>stacked</td>
<td>without</td>
<td>yes</td>
</tr>
<tr>
<td>DIG7</td>
<td>8.4µm</td>
<td>flattened</td>
<td>with</td>
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</tr>
<tr>
<td>DIG8</td>
<td>8.4µm</td>
<td>flattened</td>
<td>without</td>
<td>no</td>
</tr>
<tr>
<td>DIG9</td>
<td>2.1µm</td>
<td>stacked</td>
<td>with</td>
<td>yes</td>
</tr>
</tbody>
</table>
PROCESS VARIATIONS

Split-Lot with 9 different splits (2 wafers each split)

"NOM" → nominal case
"FAST" → MOSFETs in fast process corner
"SLOW" → MOSFETs in slow process corner
"SF" → nMOSFETs slow / pMOSFETs fast
"FS" → nMOSFETs fast / pMOSFETs slow
"HRES" → n-R max., p-R min. values
"LRES" → n-R min., p-R max. values
"LGL" → max. gate length values
"SGL" → min. gate length values
MEASUREMENT
→ TEST CHIP FUNCTIONALITY

50MHz clock
MEASUREMENT → TEST CHIP FUNCTIONALITY

FFT of digital output bitstream
MEASUREMENT

Victim $\rightarrow$ ΔΣ-DAC1 @ 50MHz  
Victim $\rightarrow$ ΔΣ-DAC5 @ 50MHz

Criteria $\rightarrow$ parasitic coupling of digital signals into analog output signal
$\rightarrow$ Spectrum analyzer @ analog AIF output

Aggressor $\rightarrow$ 1 of the other DIG circuits @ 49.5 & 50.5 MHz clock
MEASUREMENT

Difference between 50 MHz coupling and interference at 49.5 MHz

AIF output ΔΣ-DAC1

AIF output ΔΣ-DAC5
MEASUREMENT → IEC 61967 TEM CELL EME MEASUREMENT

TEM cell with mounted test board test board with DUT

→ 1 50Ω TEM cell port is terminated with 50Ω load
→ 1 50Ω TEM-cell port is connected to the input of a spectrum analyzer
→ DUT is measured four times, each time rotated by 90°
Measurement of ΔΣ-DAC1 (nominal corner) @ 50MHz, [9 kHz - 2 GHz]
Differences between the measured EME of

- DIG3 (filler cells with capacitances)
- DIG4 (filler cells without capacitances)
MEASUREMENT

→ IEC 61967 TEM CELL EME MEASUREMENT

Influence of the power ring layout between DIG2 (stacked) and DIG3 (flattened)

Again no improvement over the whole frequency range can be observed for neither variant.
CONCLUSION

- Overall recommendation:

  - Stacking the power rings to save space can be recommended, at least as long as no routing problems occur.

  - Stacking of the power rings result in no degradation considering emissions.

  - Considering emissions only, the use of filler cells with capacitances has no benefits. Although their use can be recommended as they reduce on chip interferences.
THANK YOU!