A Method to Determine Wide Bandgap (WBG) Power Devices Packaging Interconnections

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High frequency power conversion enables to reduce size and weight of power converters:

$$2\,\text{kHz}$$

$$150\,\text{W/in}^3$$

High power density of WBG devices enables to optimize packagings:

High Johnson FoM of GaN and SiC shows their abilities to operate in high power and high frequency converters:

<table>
<thead>
<tr>
<th>Johnson FoM</th>
<th>Si</th>
<th>SiC</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>FoM</td>
<td>1</td>
<td>410</td>
<td>790</td>
</tr>
</tbody>
</table>

$$JFM = \left(\frac{E_c v_{sat}}{2\pi}\right)^2$$

Accurate WBG device models including packaging characteristics are required to better predict high frequency operation of power converters.
Context

Influence of packaging interconnections for a 3-terminals transistor:

Origins of parasitics:
- Bondings
- Vias
- Pins/Pads

\( R_G, R_D \) and \( R_S \):
- Increase conduction power losses
- Slow down switchings
- Damp voltages ringings

\( L_G \) and \( L_D \):
- Gate and Drain overvoltages
- Gate and Drain voltage ringings

\( L_S \):
- Drastically increases turn on and off times
I. Calibration Procedure for S-Parameter Characterization
   1. Characterization Fixtures for the WBG Devices Under Test
   2. Open-Short Calibration
   3. Characteristics of the Calibration Fixtures

II. Access Parasitics Determination of Packaged WBG Devices
   1. SiC Schottky Diode
   2. GaN HEMT with 3-terminals
   3. GaN HEMT with 4-terminals

Conclusion
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Conclusion
I.1. Characterization Fixtures for the WBG DUT

- Transmission lines on PCB:
  - On-board SMA connectors
  - 18 GHz 500 V

- Ground plane

- FR4 Substrate ($\varepsilon \approx 4.6$)

- SiC Schottky Diode
  - IDDD04G65C6XTMA1
  - 650V / 8A

- 1-Port S-parameter characterization for 2-terminals devices:
  - $w = 3 \text{ mm}$
  - $s = 1.5 \text{ mm}$
  - $h = 1.6 \text{ mm}$
  - VNA Port 1
  - S11
  - Cathode Port 1
  - Ground Plane
  - Anode to Ground
I.1. Characterization Fixtures for the WBG DUT

- GaN HEMT with 3 terminals:

- GaN HEMT with additional Kelvin Source:

GaN HEMT
650V / 8A
GS66502B

GaN HEMT
650V / 30A
GS66508B
I.2. Open-Short Calibration

Calibration standards are required in order to get $Z$ parameters of the DUT.

$Y_0$: Coupling between line and ground plane

$Z_1$, $Z_2$, and $Z_3$: transmission lines impedances

$Y_3$, $Y_4$, $Y_5$, and $Y_6$: Coupling between transmission lines
I.2. Open-Short Calibration

Simple impedance calculations to get the Z parameter of the SiC Schottky diode

Matrix calculations to get the Z parameter of the GaN HEMT

→

→
I.3. Characteristics of the calibration fixtures

Transmission line parameters:

- $L_{TL} = 5.95 \text{ nH}$
- $C_{TL} = 2.17 \text{ pF}$
- $Z_{C_{TL}} \approx \frac{L_{TL}}{C_{TL}} = 52.4 \Omega$

<table>
<thead>
<tr>
<th>$C_4$ (fF)</th>
<th>$C_5$ (fF)</th>
<th>$C_6$ (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>52.1</td>
<td>3.09</td>
<td>203</td>
</tr>
</tbody>
</table>
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Conclusion
II.1. SiC Schottky Diode

Equivalent circuit in off-state and reverse bias:

\[ V_{AK} \]

Biasing system:

Bias Tee

Limit
II.1. SiC Schottky Diode

- Diode capacitance is characterized with this method up to 200 V
- Good accuracy for the capacitance extraction

Extracted parameters without bias:

<table>
<thead>
<tr>
<th>$R_d$ (mΩ)</th>
<th>$L_d$ (nH)</th>
<th>$C_d$ (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>442</td>
<td>7.4</td>
<td>237</td>
</tr>
</tbody>
</table>
II.2. 3-Terminals WBG Power Devices

Equivalent circuit in off-state
\( (V_{GS} = 0V, V_{DS} = 0V) \): 
\[
\begin{align*}
R_G & \quad L_G \quad C_g \quad C_d \quad L_D \quad R_D \\
C_s & \quad L_s \quad R_s
\end{align*}
\]

Inductances extraction:
\[
\begin{align*}
\text{Im}(Z_{11} - Z_{12})\omega &= L_G \omega^2 - \frac{1}{C_g} \\
\text{Im}(Z_{22} - Z_{12})\omega &= L_D \omega^2 - \frac{1}{C_d} \\
\text{Im}(Z_{12})\omega &= L_S \omega^2 - \frac{1}{C_s}
\end{align*}
\]

Equivalent circuit in Cold FET
\( (V_{GS} > V_{TH}, V_{DS} = 0V) \):
\[
\begin{align*}
\text{Im}(Z_{11} - Z_{12})\omega &\approx L_G \omega^2 - \frac{1}{C_g} \\
\text{Im}(Z_{22} - Z_{12})\omega &= L_D \omega^2 \\
\text{Im}(Z_{12})\omega &= L_S \omega^2
\end{align*}
\]
II.2. 3-Terminals WBG Power Devices

- Characterization of a SiC MOSFET in TO-247 package:

\[
\begin{array}{ccc}
L_G (\text{nH}) & L_D (\text{nH}) & L_S (\text{nH}) \\
6.96 & 0.61 & 5.82 \\
\end{array}
\]

- Characterization of the GaN HEMT G66502B:

\[
\begin{array}{ccc}
L_G (\text{nH}) & L_D (\text{nH}) & L_S (\text{nH}) \\
0.56 & 1.88 & 0.94 \\
\end{array}
\]
II.3. 3-Terminals WBG Power Devices

Access resistances extraction with the Cold FET technique:

\[
\text{Re}(Z_{11} - Z_{12}) = R_G + \frac{G_g}{G_g^2 + C_g^2 \omega^2}
\]

\[
R_G = 716 \text{ m}\Omega \rightarrow
\]

\[
\text{Re}(Z_{22}) = R_D + R_S + \frac{1}{K_1(V_{GS} - V_{TH})}
\]

\[
R_D + R_S = 172 \text{ m}\Omega \rightarrow
\]

\[
\text{Re}(Z_{12}) = R_S + \frac{1}{K_1(V_{GS} - V_{TH})}
\]

\[
R_S = 14 \text{ m}\Omega \rightarrow
\]

Extracted values:

<table>
<thead>
<tr>
<th>Component</th>
<th>Value (\text{m}\Omega)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_G)</td>
<td>716</td>
</tr>
<tr>
<td>(R_D)</td>
<td>158</td>
</tr>
<tr>
<td>(R_S)</td>
<td>14</td>
</tr>
<tr>
<td>Off-State</td>
<td>557</td>
</tr>
<tr>
<td>Cold FET</td>
<td>716</td>
</tr>
<tr>
<td>Manufacturer</td>
<td>2300</td>
</tr>
</tbody>
</table>

\(L_G\), \(G_g\), \(R_G\), \(C_g\), \(R_D\), \(L_D\), \(\alpha R_{ch}\), \(R_S\), \(L_S\), \(K_1\), \(V_{GS}\), \(V_{TH}\)
Proposed characterization method:

- Resistances: Cold FET 2-Port S-parameter measurement between G-D-PS

- Inductances:
  - 2-Port S-parameter measurement at $V_{GS} = 6V$ between G-D-PS
  - 2-Port S-parameter measurement at $V_{GS} = 6V$ between G-D-KS
  - 1-Port S-parameter measurement at $V_{GS} = 0V$ between KS-PS
II.3. 4-Terminals GaN HEMT

\[ R_D + R_S \rightarrow R_S \rightarrow R_G \rightarrow \]

- \( R_D \) (mΩ)
- \( R_S \) (mΩ)
- \( R_G \) (mΩ)

- \( L_G \) (nH)
- \( L_D \) (nH)
- \( L_{CS} \) (nH)
- \( L_{PS} \) (nH)
- \( L_{KS} \) (nH)

<table>
<thead>
<tr>
<th>( R_G )</th>
<th>( R_D )</th>
<th>( R_S )</th>
</tr>
</thead>
<tbody>
<tr>
<td>560</td>
<td>42.4</td>
<td>6.1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>( L_G )</th>
<th>( L_D )</th>
<th>( L_{CS} )</th>
<th>( L_{PS} )</th>
<th>( L_{KS} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0</td>
<td>1.3</td>
<td>0.2</td>
<td>1.2</td>
<td>1.2</td>
</tr>
</tbody>
</table>
Conclusion of the talk:

- Test fixtures and adapted calibration technique for wideband characterization
- Better accuracy of Cold FET than Off-State measurements for devices prasistics extraction
- Innovative method to characterize packaged transistors including Kelvin Source

Future work:

- Improvement on the short calibration to separate packaging from PCB connections parasitic effects
- Use of ADS software for advanced validation of the characterization method
Thank you for your attention